Semiconductor nanocrystals in dielectrics for memory purposes

Ph.D. Thesis

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Preface – motivation and objectives

Nowadays semiconductor (Si, Ge, etc.) nanocrystals embedded in dielectrics are intensively studied. One of the main goals of the researches is the exchange of conventional flash memories by nanocrystal-based flash memories.

Floating gate field effect devices are the basis of today's nonvolatile memory technology, such as the "flash" memory chips that are widely used as the data storage media in stand-alone (pen drives, memory sticks, MP3 players, PDAs, hybrid hard disks, etc.) or embedded applications (in automobiles, microcontrollers, appliances, wireless devices and other industrial controls). Information storage in these conventional semiconductor based non-volatile memories is based on the change of the threshold voltage in the case of metal-insulator-semiconductor (MIS) field-effect memory transistors, due to appropriate charging voltage pulses. During writing, charge carriers tunnel through the *tunneling layer* to the floating gate, or to the defects in the dielectric where they are stored. The presence or absence of this charge corresponds to the logical *0* or *1* states.

In accordance with the fast size shrinkage as described by Moore's law, there is an urgent need for device elements with reduced lateral dimensions, on one hand. On the other hand, protection of charge leakage from the floating-gate requires thick tunneling oxides. It implies large charging voltages that need switching circuits with large lateral sizes and hence, it is an important limitation against satisfying Moore's law. According to the 2007 edition of the International Technology Roadmap for Semiconductors, the area required for the storage of one bit information in the case of a conventional memory cell, will be 24 percent of the 2007 value 65^2 nm^2 in 2013, while the thickness of the SiO_2 layer stagnates around 8–9 nm [0−1]. This implies an increased importance of switching circuit areas which meanwhile remains the same as bottom SiO_2 layer thickness does not scale down. This is a serious technological issue, which needs to be solved.

Using semiconductor nanocrystals, charge is stored in particles separated from each other by wide band-gap dielectrics. This increases reliability because a single nanocrystal cell does not lead to complete charge loss as through an occurring defect in the case of a conventional floating gate. The use of nanocrystals is thus expected to be a promising alternative to the present floating gate technology. The conclusion, that it is a valid solution for the limitation issues of conventional technology, is confirmed by the fact that IBM reported the first nanocrystal memory device in 1996, and this was followed by Motorola's demonstration of a 4 Mbit Si nanocrystal memory device in 2003.

The main objective of my Ph.D. work was the experimental study of the preparation and operation of metal–insulator–semiconductor (MIS) capacitance structures with embedded Si or Ge nanocrystals. The preparation of such structures involved low-pressure chemical vapour deposition, electron beam evaporation and nitric acid oxidation (the latter was applied to Si nanocrystals for the first time). The size, density and location of these nanocrystals was varied to optimize the memory properties (charge injection and charge storage). Size-dependent structural parameters on the nanocrystalline structures (mainly the nanocrystal size, density and separation, and the thin film thickness and composition) were determined by a variety of investigation methods, such as spectroscopic ellipsometry, cross-sectional transmission electron microscopy (XTEM), atomic force microscopy (AFM), scanning electron microscopy (SEM), X-ray photoelectron spectroscopy, and sheet resistance measurements.

Intensive research in recent years enabled the embedded nanocrystal structures to become suitable for the low charing voltage needs (below 10 V) of the non-volatile industry. However, numerous physical aspects of the device operation is still not clear: e.g., whether the charge is stored in quantum states of a nanocrystal quantum box or in defect states at the nanocrystal/dielectric interface. There is only scant data about the charge distribution in the layer in the presence of nanocrystals as well. My contribution to the topic was, on one hand, the electrical memory investigation of such structures, as a function of structural parameters of the embedding layers and the nanocrystals, and on the other hand, the structural investigations of nanomaterial systems, which itself bears also important challenges. For example, the absence of reference dielectric spectra for the optical models of nanocrystalline materials is a considerable deficiency. That is why spectroscopic ellipsometry was applied for the parametric composition of the dielectric function of nanocrystalline silicon.

My motivation in this work was to contribute to this topic with new designs of structures, deep investigation of nano-material properties, and optimization of the structure design according to electrical memory qualifications.

This Ph.D. thesis is organized as follows:

Chapter 1 presents a classification of electronic memories and an introduction to the preparation and to the memory application of embedded Si and Ge nanocrystals in dielectric layers.

In Chapter 2, the preparation methods used in this work for both the nanocrystals and the dielectric layers are described. The design considerations and the summary of prepared samples is also discussed here. This is followed by Chapter 3, which summarizes the applied investigation methods including the optical models for spectroscopic ellipsometry, and the method of memory measurements.

Chapter 4 discusses the main results of the structural investigations of the studied structures. The results of cross-sectional transmission electron microscopy, X-ray

photoelectron spectroscopy, atomic force microscopy, scanning electron microscopy, spectroscopic ellipsometry, and the sheet resistance measurements are summarized here.

Finally, in Chapter 5, the main results of the memory measurements are discussed, including the results of the capacitance–voltage hysteresis, the memory window, and the charge retention measurements.

Chapter 1 – Introduction to non-volatile memories

1.1 Classification of electronic memories

Semiconductor memories are essential elements of present day electronic devices. Such devices are used in pen-drives, memory cards, MP3 players, personal digital assistants (PDAs), general positioning system (GPS) and robotic systems or in mobile phones. Commercially available electronic memory devices (and also those that are under development) can be distinguished by some basic properties which are the following.

1. Volatility. Volatile memories lose information if they loose power, while non-volatile memories store information without supplying power. The two most common volatile memory types are dynamic random access memory (DRAM) and static random access memory (SRAM). DRAM needs to be periodically refreshed, while SRAM keeps information without any refreshment until power remains applied. They typically need low programming voltages (around 1 V) with ultra-small times required for programming (in the range of 10–50 ns) [0–1]. Non-volatile memories need higher programming voltages (in the range of 7-19 V) with a wide range of reported programming times, between 50 ns and 100 ms [0–1].

2. Method of information storage. As volatile memories are off-topic to present subject, only non-volatile memories are dealt with in the following. Among non-volatile memories, a variety of used information storage mechanisms exist.

2.a. Non-charge-storage memories

- *Ferroelectric memories (FRAMs)* use ferroelectric layer as a dielectric inside a capacitor for information storage. They need small and short programming voltage pulses like volatile memories, and indeed, in construction they are similar to DRAM. This memory technology features advantages of high-speed data read/write functions, low power consumption, and virtually unlimited read/write cycles [1–1].

- *Magnetoresistive memories (MRAMs)* also use a capacitor in the memory cell but the ferroelectric element is not in the dielectric, but in the plates instead. They also need low and short voltage pulses for programming [1–1].

- In the case of *phase-change memories (PRAMs)* the phase of a channel is switched by voltage pulses between nanocrystalline and amorphous state (that corresponds to high and low conductance, respectively). The best published programming voltage pulse amplitudes are extremely low (below 1 V) and the required pulse width is also in the range of 50 ns. Phase-change memories are widely thought to be the final alternatives to replace present-day non-volatile memories, and to become the "ultimate memory". However, if using as devices, more dramatic change is needed for them in the technological process comparing to present-day flash memory structures, than

for nanocrystal flash memories. Nevertheless, nanocrystal flash memories seem to be a good temporary solution until phase-change technology reaches the level demanded by solid-state manufacturers. [1−1]

2.b. Charge-storage memories

– The *Electrically Erasable Programmable Read Only Memory (EEPROM)* was introduced in the early 80's. Unlike its earlier version, EPROM, it can be reprogrammed by applying an electrical voltage. As a matter of fact, EEPROM is erased and reprogrammed at the individual cell level. While this results in high functionality which makes it well suited to particular applications for program memory of embedded systems, EEPROM devices are generally less cost-effective and are slower to program and erase than flash memory devices. However, they are ideal for the storage of firmware code because of the possible access at the byte-level. [1−1]

– The *flash memory* is currently the largest segment of the non-volatile memory market and is similar to EEPROM in that it can also be erased and reprogrammed repeatedly through the application of an electrical voltage. Flash memory cells can be erased in blocks by a single action or "flash", which makes it cost far less because of the simplified design, than EEPROM. Their programming voltage amplitudes are currently typically between 7 and 19 V. [0−1,1−1]

1.2 Materials and methods of preparation

A silicon nanocrystal based memory structure was first suggested and published by Sandip Tiwari et al. from IBM Research Division, in Applied Physics Letters on 4th March 1996 [1−2], which became the most cited article ever published on this subject. His group realized an n-channel silicon FET with a sheet of Si nanocrystals (NCs) distributed in a silicon dioxide film, above the channel. They used a very thin tunneling oxide (1.1–1.8 nm) and a thicker control oxide above the NCs (4.5 nm or thicker).

NC-based electronic non-volatile memory structures are prepared by four main methods, that are described in this chapter. These are: the ion-beam synthesis, the layer-by-layer growth, the non-stoichiometric layer deposition and the CVD method.

From the application point of view, the *ideal NC size, density and position* inside the dielectric medium is crucial. It is important *to position the NCs to a 2-3 nm distance from the Si substrate*, on top of a good quality SiO_2 to enable direct tunneling from the substrate to the NCs. The Si/SiO_2 interface must be as perfect as possible to minimize the density of trap sites on the interface and to avoid its influence on the formation of accumulation and inversion layer during application of voltage to the device.

On one hand, the *NC size must be larger than 3–4 nm* because of the effect of charge confinement, namely: the increase of energy levels when more than one electrons are stored. This would badly affect charge retention characteristics since the potential

barrier for the electron occupying the highest energy level would decrease in this case comparing to NCs with larger size as the energy level separation increase according to the following equations [1−3]:

$$C_{NC} = 2\pi\varepsilon d \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad (Eq.\ 1-1)$$

$$\Delta E_{n,n-1} = \frac{q^2}{2C_{NC}}(n^2 - (n-1)^2) = n \cdot \frac{q^2}{C_{NC}} - \frac{q^2}{2C_{NC}} \qquad\qquad (Eq.\ 1-2)$$

where d is the diameter of a spherical NC, C_{NC} is the capacitance of a spherical NC and $\Delta E_{n,n-1}$ is the separation between energy levels inside the NC.

On the other hand, *NC density at least 10^{12} cm^{-2} is required* to minimize statistical variations. As the *typical separation of NCs must be greater than 4 nm (to minimize lateral tunneling between NCs), NC size around 5 nm could be optimal.* [1−3] An additional requirement for the NCs is that their size distribution must be narrow enough to avoid statistical effects which block further application in real memory devices.

1.2.1 Ion beam synthesis

The most frequently used method is the ion beam synthesis, which means implantation of Si or Ge into a SiO$_x$ layer with ultra-low-energies and subsequent annealing (or oxidation) at high temperatures. In the next few paragraphs, some examples of recent and typical achievements are summarized. A comprehensive list of publications in such subject is available on http://www.cemes.fr/neon.html that is the homepage of a former EU project called NEON (Nanoparticles for Electronics).

Si nanocrystals

Formation of Si NCs takes place after implantation typically with dose of 10^{15}–10^{16} ions/cm^2. The size of the NCs can be controlled between approximately 2–15 nm by adjusting the post-annealing temperature around 1000°C. A few examples from the literature are described below.

Normand et al. [1−4,1−5] implanted Si$^+$ ions at 1 keV with a dose in the order of ~10^{16} ions/cm^2 into 7–8 nm thick thermal SiO$_2$. They observed Si nanoclusters with sizes in the range between 4–14 nm by TEM depending on the annealing temperature, which was ranging from 900°C to 1000°C for 30 or 60 min in N$_2$.

Heinig et al. [1−6] implanted their 15 nm thick thermal SiO$_2$/Si structure with Si$^+$ ions at 50 keV with a dose in the order of ~$3 \cdot 10^{15}$–10^{16} ions/cm^2. They predict Si NCs with 2–3 nm diameter by Monte-Carlo simulation, however, they did not observe them with XTEM because of the too small size. Their annealing procedure was executed at temperatures between 950–1100°C and times between 5–180 sec in inert ambient. Both authors suggest that Si NC formation takes place basically because of phase separation of Si and SiO$_2$ during annealing.

Ge nanocrystals

In the case of Ge NC formation, doses between 10^{15}–10^{17} ions/cm^2 are typically used. The post-annealing temperature needed to form the nanoparticles is somewhat lower than in previous case, here it is around 600°C. Two typical experiments are reviewed below.

Tsuji et al. [1−7] implanted Ge$^-$ ions at 10 keV with a dose in the order of (1–5)·10^{15} ions/cm^2 into 12 nm thick thermal SiO$_2$. They observed Ge nanoparticles with sizes in the range between 2–5 nm by cross-sectional transmission electron microscopy (XTEM) depending on the annealing temperature and implantation flux, which was ranging from 300°C to 900°C for 60 min in vacuum. They found that thermal diffusion of Ge atoms in SiO$_2$ is notable in the case of annealing at 900°C, however, it was negligible at 300°C.

Masuda et al. [1−8] implanted Ge$^+$ ions at 8 keV (low energy implantation, LEI) or 50–360 keV (high energy implantation, HEI) with a dose in the order of 10^{16}–10^{17} ions/cm^2 into thick SiO$_2$ films. They observed Ge nanoparticles with 4.5 nm average diameter in the case of HEI and 5.2 nm in the case of LEI by transmission electron microscopy (TEM). The annealing was executed with temperature of 600°C for 30 min in N$_2$. They found by Rutherford backscattering spectrometry (RBS) that there is no significant compositional difference between the as-implanted sample and the annealed sample.

Si and Ge nanocrystals

Unexpectedly, both Si and Ge NC formation were observed by Giri et al. [1−9] with Ge implantation only, after annealing at higher temperatures, between 800 and 950°C.

Giri et al. [1−9] implanted Ge$^+$ ions at 300 keV with a dose in the order of 3·10^{16}–2·10^{17} ions/cm^2 into 250 nm thick thermal SiO$_2$. They observed both Si and Ge nanocrystals after annealing in argon at 800°C and 950°C for several hours. Ge NCs sizes were found to vary between 4 and 13 nm estimated from Raman scattering data depending on annealing temperature and implantation dose. They obviously found that increasing the annealing temperature results in the increase of NC size. They estimate the average size of Si NCs which were identified by optical Raman spectra, for 8 nm by XRD, however, they expect that Si NC sizes are smaller than that of Ge's because of smaller Si concentration present in the layer.

1.2.2 Layer by layer growth

Another method is a layer by layer growth, i. e., the deposition of a thin amorphous or polycrystalline Si or Ge layer onto a lower dielectric (SiO$_2$, Si$_3$N$_4$, etc.) layer. This Si or Ge layer is either covered by another dielectric layer, or the Si grains themselves are oxidized. The nanocrystals are formed by annealing either during evaporation, after the deposition of the Si or Ge layer, or after the deposition of the second dielectric layer.

Such structure was prepared by Kobayashi et al. [1−10] who evaporated a thin, 10 nm thick Ge layer onto a 4-nm-thick thermal SiO$_2$ by e-beam evaporation at a substrate

temperature of 60°C at 10^{-7} Torr high vacuum. The sample was then annealed at temperatures between 800 and 1000°C in O_2 atmosphere. Due to this high temperature oxidation, the Ge became oxidized and formed NCs with average sizes of 5 nm as obtained by modeling the measured Raman line shape. They monitored the Ge position by secondary ion mass spectrometry (SIMS) after oxidation and found that Ge stays on top of the bottom oxide in the case of oxidation at 800°C, while oxidation at 1000°C caused diffusion of the Ge content to the interface of Si/SiO_2.

Note, that it is in correspondence with the result found by Tsuji et al. [1−7] described above, who found that diffusion of Ge atoms is notable in the case of annealing at 900°C.

However, another article reports different result. Shklyaev et al. [1−11] published that e-beam evaporation of Ge onto thin SiO_2 covered Si substrates with growth temperatures between 320 and 430°C results in Ge island growth on the SiO_2 layer, while growth temperatures between 430 and 600°C drive different mechanism. At this temperature regime, epitaxial growth takes place on the a-SiO_2 layer which can be possible if the Si surface becomes visible for the incoming Ge atoms. It means that part of the oxygen content of the SiO_2 leaves the Si surface as SiO and GeO. This is partly in contradiction with the statement in previous article, namely, that Ge stays on the surface of thin SiO_2 at oxidation temperatures around 800°C. As a matter of fact, this temperature is far higher than 600°C, but the ambient is O_2 in that case that could be responsible for the absence of oxygen reduction of SiO_2 by Ge. Another point is that in former case the thickness of the evaporated Ge layer was around 10 nm, while Shklyaev et al. deposited Ge layers with thicknesses between 1–7 monolayers.

Another article reports several temperature dependant pathways for the Ge species on SiO_2 [1−12]. Based on this, for temperatures above 500°C, the following three-step process is suggested for the Ge to evaporate:

1. $Ge(s) + SiO_2 \rightarrow GeO_2(s) + SiO_x$
2. $GeO_2(s) + Ge(s) \rightarrow 2GeO(s)$
3. $GeO(s) \rightarrow GeO(g)$.

In summary, as a result of high-temperature treatment, Ge nanoparticles on thin SiO_2 layers either diffuse to the interface of Si/SiO_2 or leave the solid phase as gaseous GeO.

1.2.3 Non-stoichiometric dielectric layer deposition

The third method is the deposition of a Si-rich or Ge-containing SiO_x or SiN_x layer, and formation of nanocrystals within the SiO_x or SiN_x layer by high temperature annealing [1−13].

As an example of this method for formation, I would mention the work of Iacona et al. [1−13] who used PECVD to deposit Si-rich SiO_2 films. They found NC formation due to high temperature annealing (between 1000–1300°C). Transmission electron microscopy (TEM) study revealed NCs with mean diameters between 1.4 and 4.2 nm.

1.2.4 Direct CVD growth

The fourth, most recent method is the deposition of Si nanocrystals themselves or of a SiN_x layer containing Si nanocrystals by different chemical vapor deposition (CVD) methods. An important point is the *control of initial nucleation of Si NCs* on top of SiO_2.

Brunets et al. [1−14] create reactive surface sites on the oxide by changing the surface Si–O bonds with Si–OH (silanol) bonds with the use of a solution of 0.3% HF and 0.3% HCl. Silanol bonds have significantly lower dissociation energy which means that the incoming Si atoms could more easily break the silanol bond and bond to the SiO_2. The same method was applied by Baron et al. [1−15], however, Rao et al. [1−16] did not use similar procedure.

Brunets et al. [1−14] deposited Si NCs by LPCVD on top of 2.5 nm thick SiO_2 covered Si substrates at temperatures around 300°C using disilane and trisilane source gases. The nanocrystal formation took place directly during deposition and their typical diameter was found to be around or below 5 nm. Finally, the samples were covered with atomic layer deposition (ALD) of Al_2O_3.

Baron et al. [1−15] also used LPCVD for the formation of Si NCs but with silane and dichloro-silane as input gases. They proposed a two-step model for the CVD process: first, a nucleation step takes place with the introduction of silane to the system, and second, the growing of Si *nuclei* with dichloro-silane as precursor. They obtained a direct correlation between deposition time of the second step (0–50 min) and Si NC size (0–30 nm) by atomic force microscopy (AFM) measurements.

Rao et al. [1−3,1−16] used LPCVD for Si NC deposition on SiO_2 covered Si substrates and obtained Si NCs with sizes around 5 nm and density of 10^{12} cm^{-2}.

Sung et al. [1−17,1−18,1−19 used PECVD to deposit embedded Si NCs in amorphous SiN_x layers with total pressure, plasma power, and growth temperature around 0.5 Torr, 5 W, and 250°C, respectively. They observed Si NCs with diameters between 2.6 and 6.1 nm as varying the deposition parameters. No annealing was required for the NC formation.

Wan et al. [1−20] used LPCVD to directly deposit Si NCs with a silicon nitride shell (they refer to the structure as SiN »silicon nitride« dot). They use LPCVD with dichloro silane (DCS) and ammonia (NH_3) at 725°C and DCS/NH_3 ratio of 1/5 and found that during initial stage of stoichiometric Si_3N_4 deposition, the layer is not continuous and Si-rich. As nitride growth begins with creation of Si-to-Si bonds, they explain slower growth on silicon oxide substrates than on silicon substrates. They interrupted the deposition at a certain time and expected that Si nanodots would not be continuous laterally, surrounded by silicon nitride shells.

1.3 Memory characterization of flash memory structures

1.3.1 Principles of operation

Information storage in conventional flash memories is based on the change of threshold voltage of field-effect transistors (FETs) by appropriate voltage pulses. During writing to the device, charge carriers tunnel to the "floating gate" where they are being stored. Reading procedure is based on applying a low voltage to the gate of the FET and check by measuring the source-drain current whether it is opened. Future applications such as the use in notebooks instead of hard disks require smaller and faster memory device elements which operate with lower voltages. However, the reduction of dimensions is limited in the case of conventional flash memories. Replacing the continuous floating gate by isolated nanocrystals is a possible new technology, which replaces conventional devices. A schematic of a nanocrystal-based flash memory transistor is shown in *Fig. 1−1*. In the case of leakage, only a part of nanocrystals would deplete and the information is retained. It implies the possibility of smaller voltage pulses, as smaller charge amount is enough to be present in the layer to provide reliable information storage.

S. Tiwari et al. [1−2] describe the information storage mechanism in such device as follows. The injection of electrons takes place by direct tunneling from the inversion layer to the NCs by applying reverse bias to the gate. As a consequence, the stored charge screens the gate charge that results in the reduction of conductance in the inversion layer, i.e., it effectively shifts the threshold voltage of the device. They suggest a device with NC sizes of 5 nm with separation of 5 nm (corresponding to density of 10^{12} cm^{-2}), and top oxide thickness of 7 nm. With this structure, the threshold voltage shift is around 0.3–0.4 V for one electron per NC whose effect can be easily detected by source-drain current measurement. The Coulomb blockade energy for such NC is around 74 meV that is on one hand, larger than the room temperature thermal energy, and on the other hand, enables multi-electron storage in a single NC.

It is essential to minimize the writing/erasing (W/E) voltage amplitudes of the devices. So, a key issue is the optimization of the structure for maximizing the injection current at a given gate voltage. The injection current is essentially an exponential function of the electric field in the bottom dielectric layer [1−21]. The bottom dielectric layer is often referred as the tunneling layer, or the tunneling oxide layer (in most cases, it is a SiO$_2$ layer on top of the Si substrate). The electric field in this tunneling layer is a function of the thickness of this layer, the thickness of the top dielectric layer, the dielectric constants of both layers, and the trapped charge in both layers. When no charge is stored in the structure, the electric field in the tunneling oxide layer is given as

$$E_{ox} = \frac{V_{gate}}{x_{ox}\left(1 + \frac{\varepsilon_{ox} \cdot x_n}{\varepsilon_n \cdot x_{ox}}\right)},$$ *(Eq. 1−3)*

where V_{gate} is the gate voltage, ε_{ox} and x_{ox} are the dielectric constant and the thickness of the bottom oxide layer, respectively, and ε_n and x_n are the dielectric constant and the

thickness of the top layer, respectively [1−21]. This suggests that the decrease of the $\frac{\varepsilon_{ox}}{\varepsilon_n}$ ratio increases the oxide field, and this increase is independent of the gate voltage. Practically, this means that the dielectric constant of the top dielectric layer should be larger than that of the bottom layer. Such a case is achieved in metal-nitride-oxide-silicon (MNOS) structures, because the dielectric constant of the Si_3N_4 is between 6.9–7.5, while the dielectric constant of SiO_2 is around 3.9 [1−1].
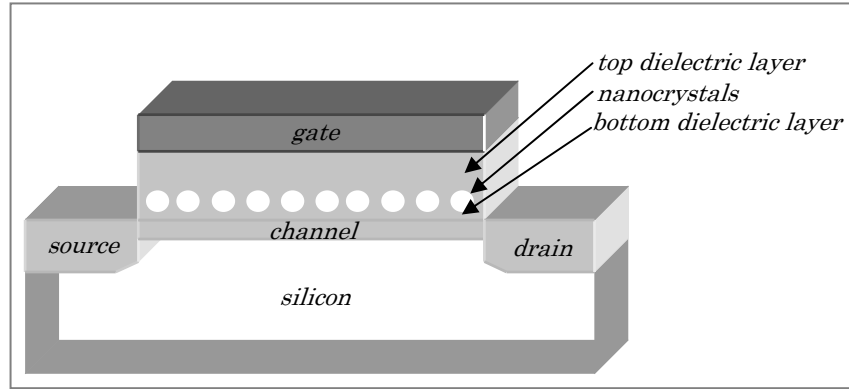
Fig. 1−1. Flash memory transistor with nanocrystals

The energy band diagram during charge injection for a MNOS capacitor with Si nanocrystals is shown in *Fig. 1−2*. Charge is injected from the accumulation layer in the substrate to either the NCs or to defect sites (traps) located in the Si_3N_4 layer by tunneling. Direct tunneling takes place if the underlying oxide layer is sufficiently thin enough (~3 nm).

After injection, the total stored charge in the nitride layer is given by

$$Q = q \cdot \int_{x_{oxide}}^{x_{nitride}} n(x)dx, \qquad\qquad\qquad (Eq.\ 1\!-\!4)$$

where q is the elemental charge, $n(x)$ is the spatial distribution of charge, and x_{oxide} and $x_{nitride}$ are positions in the layer, as shown in *Fig. 1−2*. In the case of calculations for metal-oxide-semiconductor (MOS) structures, it is often approximated that the stored charge is located at the Si/SiO_2 interface, because the function $n(x)$ is usually not known. However, for charge trapped in MNOS structures, the *charge centroid* is defined [1−22,1−23,1−24,1−25] which describe this distribution by the position of the centroid in the nitride. It is generally defined as

$$x_c = \frac{1}{Q} \cdot \int_{x_{oxide}}^{x_{nitride}} x \cdot n(x)dx, \qquad\qquad\qquad (Eq.\ 1\!-\!5)$$

where x_c is the distance of the charge centroid from the Si/SiO_2 interface, and Q is the total stored charge in the layer.
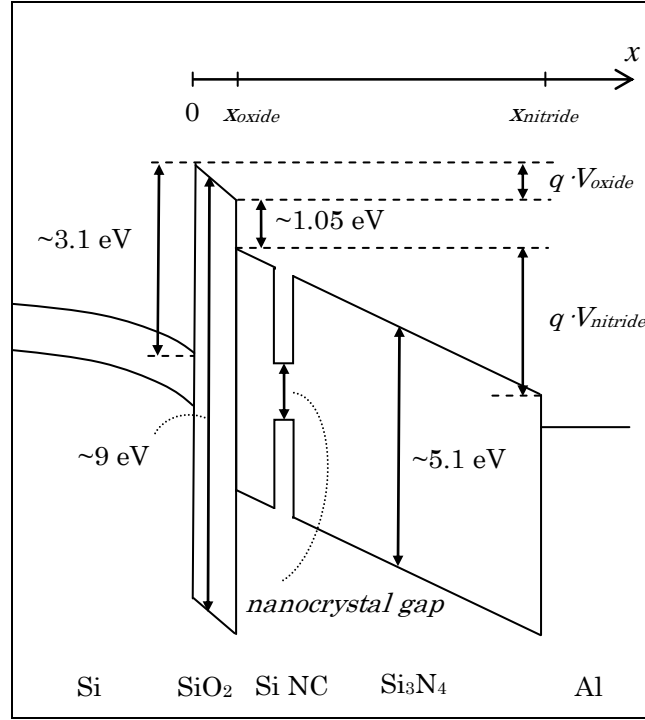
Fig. 1–2. A schematic of the energy band diagram during charge injection for a MNOS capacitor with Si nanocrystals

The flat-band voltage in metal-insulator-semiconductor (MIS) devices is the voltage at which there is no electrical charge in the semiconductor and, therefore, no voltage drop across it; in the band diagram the energy bands of the semiconductor are horizontal (flat) [1–26]. The flat-band voltage V_{FB} in an MNOS structure is generally given by

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_n}\left(x_n + \frac{\varepsilon_n}{\varepsilon_{ox}}x_{ox}\right) - \frac{Q_n}{\varepsilon_n}(x_n - x_c), \qquad\qquad (Eq.\ 1\text{–}6)$$

where ϕ_{ms} is the work function difference between the metal (usually Al, or poly-silicon) and Si, Q_n is the density of charge (per unit area) stored in the nitride layer (including the NCs) with thickness x_n, Q_{ox} is the charge density in the oxide, if it is at the Si/SiO$_2$ interface, x_{ox} is the oxide thickness, and ε_n and ε_{ox} are the dielectric constants for the nitride and the oxide layer. However, in practice Q_{ox} is negiligible and the corresponding term can be neglected. Consequently, the flat-band voltage shift caused by the injected charge density ΔQ_n in the nitride layer (including the NCs) is then given as

$$\Delta V_{FB} = \frac{1}{\varepsilon_n}(x_n - x_c)\Delta Q_n, \qquad\qquad (Eq.\ 1\text{–}7)$$

This means increased effect of the trapped charge on the memory window width if it is located closer to the substrate (it is characteristically at the SiO$_2$/Si$_3$N$_4$ interface if x_c equals zero). As NCs (representing large density of traps) are formed directly at the SiO$_2$/Si$_3$N$_4$ interface (in the case of MNOS structures), improvement of the memory window is expected for MNOS samples with embedded NCs, with respect to MNOS reference samples (without the NCs).

In the case of structures where only NCs are considered to store the charge (e.g. NCs embedded in SiO₂), if only one electron per NC is assumed, the following equation is obtained (by deriving Poisson's equation in an oxide) for the resulting flat-band voltage shift [1−27,1−28,1−29]:

$$\Delta V_{FB} = \frac{1}{\varepsilon_{ox}} \cdot \left(x_{ox} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{NC}} d_{NC} \right) \cdot \Delta Q_{NC},$$

(Eq. 1−8)

where ε_{NC} is the effective dielectric constant of the nanocrystal, d_{NC} is the diameter of the NCs, and x_{ox} is the thickness of the oxide layer above the NCs.

Combining *Eq. 1−7* and *Eq. 1−8*, in the case of MNOS samples with embedded NCs in the nitride close to the SiO₂/Si₃N₄ interface, the following relation is obtained:

$$\Delta V_{FB} = \frac{1}{\varepsilon_n} \cdot \left[(x_n - x_c) \cdot \Delta Q_n' + \left(x_n + \frac{\varepsilon_n}{\varepsilon_{ox}} x_{ox} \right) \cdot \Delta Q_{NC} \right],$$

(Eq. 1−9)

where Q_n' is the density of charge stored in the nitride only (excluding the NCs).

During charge storage in our case, the single MIS capacitor device is separated from the charging circuit by a relay immediately when the charging voltage returns to zero. Then discharge phenomena occurs by tunneling from either the NCs or the nitride traps backwards to the substrate or in forward direction, towards the top electrode. The discharge current is strongly determined by the barrier height for the tunneling carriers which is a definite function of the NC size [1−30], by the density of the NCs, and by the total stored charge [1−29]. The amount of charge stored in the device [1−29,1−32] is given as

$$\frac{dQ}{dt} = -P(t) \cdot Q(t)$$

(Eq. 1−10)

$$Q(t) = Q(0) \cdot e^{-\int P(t)dt},$$

(Eq. 1−11)

where $P(t)$ is the transition probability of a charge carrier from a trap state to the substrate, which is given as

$$P(t) = \int_{E>E_c} \nu_{NC} \cdot \rho(E) \cdot T_m(E) \cdot e_n(E_t) \cdot \beta \cdot dE.$$

(Eq. 1−12)

Here, $\rho(E)$ is the density of states, $T_m(E)$ is the transmission probability across the bottom oxide, $e_n(E_t)$ is a temperature-dependent factor, β contains the geometry, and ν_{NC} the semi-classical escape attempt rate for NCs, which is given as

$$\nu_{NC} \approx \frac{h}{4 m_{NC} d_{NC}^2}.$$

(Eq. 1−13)

Here, m_{NC} is the effective electron mass in the nanocrystal, and d_{NC} is the NC diameter [1−29,1−31].

1.3.2 Definition of the memory window

The written state of a memory capacitor structure is defined by its flat-band voltage after the application of a high voltage pulse (where "high" means higher than the voltage used during the "read" procedure) to the structure. The erased state is defined by the flat-band voltage after the application of an opposite voltage pulse. The *memory window width* of a memory element is defined by the flat-band voltage difference between the written and the erased state. The *position of the memory window* is defined as the value of the flat-band voltage.

1.3.3 Definition of the retention

Basically, the charge retention of a structure is given by the change of its flat-band voltage after a single W/E voltage pulse, as a function of waiting time. The retention is often characterized by the extrapolated value of the memory window width for 1 or 10 years. This extrapolation is based on the exponential time dependence of the amount of charge in the device (see *Eq. 1−11*).

1.3.4 Recent results

Recent results reported on memory devices with Si nanocrystals prepared by ultralow-energy ion-beam synthesis are promising [1−5,1−33]. It was obtained that the memory behavior of the devices prepared by this method does depend not only on the implantation (energy and dose) and annealing (temperature, time, ambient) parameters, but also on such effects and circumstances, as contamination and electrical charging of the sample surface during implantation, oxide swelling, cleaning procedure before annealing, and the energy contamination [1−5].

Optimizing the above parameters, memory transistors with the following characteristics were obtained by Normand et al. [1−5]. About 2 V memory window width was obtained for W/E pulses of ±9 V, 10 ms. No change of the memory window was detected after 1.5 million W/E cycles (stress). The extrapolated memory window of unstressed devices kept at 85°C is 0.4 V after 10 years, it means that the memory window decreased to ~20% of its initial value. The stressed devices also store the information for several years.

In another recent work of Ng et al. [1−33] memory window width of about 1 V has been achieved by writing/erasing pulses of ±12 V, 1 µs on devices prepared also by ultra-low-energy ion-beam synthesis. The extrapolated memory window width after 10 years is about 0.3 V.

Another important result is the realization of MOS memory FETs with Si nanocrystals feasible for dual bit storage of information [1−34]. In another work the effect of single electron charging on the drain current was demonstrated and studied in detail [1−35].

1.3.5 Recent solutions on the market

Since Freescale Semiconductors (a spinoff company of Motorola) introduced a 4-Mbit nanocrystal flash memory in production in 2003, and a 24-Mbit array in 2005 [1−36,1−37], development effort in nanocrystal memory cells is ongoing with at least 5 of the top 10 flash memory suppliers [1−38].

Developers and vendors of nanocrystal memories include among others Atmel, Freescale (Motorola), IBM, Renesas, Toshiba, or Hitachi. According to an analysis, the flash memory market (with the conventional floating-gate flash memory transistors) is expected to double between 2005 and 2009, worldwide [1−39]. A recent report in Hungary revealed that the growth of the local flash memory market doubled from 2006 to 2007 [1−40].

Freescale

This company has created the world's first 24-Mbit memory array using 90 nm CMOS bulk technology. They state that the production of a working 24-Mbit memory device requires that silicon nanocrystals be deposited with good uniformity and integration approaches that keep the nanocrystal properties intact during subsequent processing. In successfully achieving this, Freescale has overcome major challenges to introducing this technology into production.

They created nanocrystal memory cells by forming a layer of 5 nm silicon dots, deposited on a 5 nm grid on top of the thin gate oxide layer. Another oxide layer is deposited on top of the nanocrystal layer, and then the polysilicon gate is formed on top of the oxide. As the tunnel oxide under the nanocrystal layer can be scaled down, reducing the voltage needed for program/erase operations: 8 to 10 V, as opposed to the 12 to 15 V used for most floating-gate storage cells.

Atmel Corp.

Atmel has an on-going R&D project for next generation non-volatile memories, called Erevna. The overall objective of this project is to develop flash memories with embedded silicon nanocrystals at the 130-nm, 90-nm, and 65-nm nodes, for use up to the year 2009. [1−41]

Spansion

The company Spansion was founded as a result of agreement between Fujitsu and AMD in 1993. It is currently one of the largest vendors of flash memory devices. However, there is no data about its production of nanocrystal flash memories, its fellows publish scientific results about the subject in the literature [1−42,1−43].

Other companies

Members of staff of the other big companies, such as Hitachi [1−44], IBM [1−45] or Toshiba [1−46] are also publishing on nanocrystal flash memories, however, there is no data available about implementing their results into production.

1.4 Conclusions

In this chapter, a brief introduction was given into the subject *non-volatile memories*. A grouping of electronic memories was presented, from the view-points of volatility and method of information storage. Common materials and methods of preparation were reviewed, with a comparison between different observations in the literature. Emphasis was taken on the formation of Si and Ge nanocrystals in dielectric layers. Memory qualification methods of flash memory structures were shown, with the principles of operation. The theoretical background for charge storage is introduced. The definition of the *memory window* and the *retention* was explained. A summary of recent flash memory products with nanocrystals was showed.

Chapter 2 – Methods of preparation of the studied structures

2.1 Introduction

The experimental procedures used in this work are described for different layer depositions, and for the formation of Si or Ge nanocrystals in the followings.

2.2 Preparation of thin layers

2.2.1 Silicon nitride layers

Low-pressure chemical vapor deposition (LPCVD) method provides a trustworthy way of depositing electrically insulating silicon nitride thin layers. However, other methods such as sputtering or plasma-enhanced chemical vapor deposition (PECVD) exist, these are not operated at low pressures, low activation energies, or the reagents are too large during deposition, and hence, the resulting layer is not dense nor defect-safe enough to provide low leakage currents during electrical applications.

In this work, the setup used for the deposition of silicon nitride thin layers was a software-controlled Amtech-Tempress LPCVD device. It operates at 30 Pa pressure and a temperature of 810^OC is used regularly for silicon nitride processing. The silicon nitride layers are formed on top of (100) oriented Si wafers as introducing SiH_2Cl_2 (dichloro-silane, or *DCS*) and NH_3 into the heated quartz tube according to the following equation:

$$SiH_2Cl_2 + NH_3 \rightarrow Si_3N_4 + HCl + H_2 + NH_4Cl .$$ *(Eq. 2–1)*
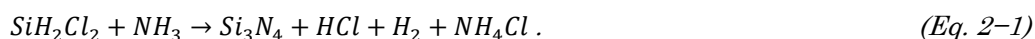
The stoichiometric layers were grown with gas flow rates of DCS to NH_3 of 21 to 90 sccm, respectively. For non-stoichiometric layers, the DCS to NH_3 ratio was increased.

The thickness of the layer was controlled by the deposition time and verified by spectroscopic ellipsometry measurements on reference samples. The obtained deposition time vs. thickness data is plotted in *Fig. 2–1*. The actual growth speed of the layer is found to be around 3.9 nm/min below 10 min, and around 1.6 nm/min above 10 min. The difference of layer growth speeds is probably connected with the relatively slow (around 30 sec) switch-on time of the DCS cock, that strongly affects the incubation time of the growth process. Later, the deposited layer thickness is clearly a linear function of the deposition time.
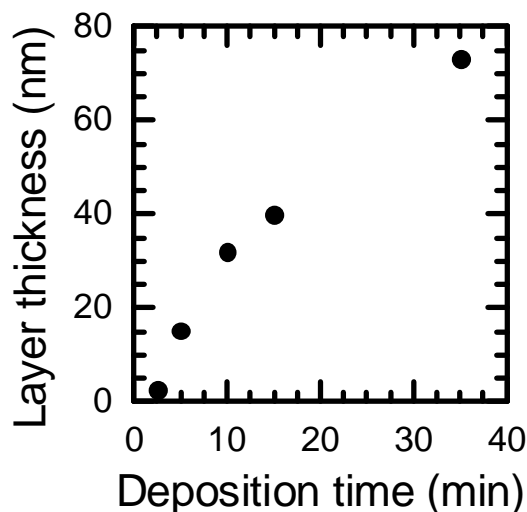
Fig. 2−1. Deposition time versus Si_3N_4 layer thickness in the case of LPCVD growth

2.2.2 Thin silicon dioxide layers

For the formation of thin silicon dioxide layers, a method by use of HNO_3, as reported earlier by H. Kobayashi et al. [2−1] was applied after cleaning the (001) oriented n-type Si substrates in 1 wt% HF. Then, the n-type Si wafers were immersed in 68 wt% HNO_3 at the boiling temperature (121 °C) for 60 minutes. This method yielded a SiO_2 layer with a thickness of 2.5 nm, as obtained by cross-sectional transmission electron microscopy (XTEM).

2.2.3 Thick silicon dioxide layers

Thick (~100 nm) SiO_2 layers were formed either by thermal oxidation of Si or by atmospheric chemical vapor deposition of SiO_2 with SiH_4 and O_2.

2.3 Preparation of nanocrystals

2.3.1 Si nanocrystals

Si nanocrystals were formed during LPCVD with single SiH_2Cl_2 input gas at 30 Pa pressure and temperature of 810°C. Thin layers of nanocrystalline Si were prepared with deposition times between 30 sec and 300 sec on Si_3N_4, SiN_x and on SiO_2 covered Si substrates. The initial expectation was, that below a certain deposition time, the resulting thin layer becomes non-continuous. Note, that it was one of the goals of the work for this thesis.

I suggest here a discrete definition of terms *Si nanocrystalline layer* and *Si nanocrystals*. In the followings, I mean a continuous layer of silicon with small crystalline grains (with grain sizes in the *nano* range) as a *Si nanocrystalline layer* (nc-Si). As for *Si*

nanocrystals (Si NCs), I would call nanocrystals (with sizes in the *nano* range) that are separated from each other by a material other than Si.

It is emphasized here, that the size of Si nanocrystals could be reduced by post-oxidizing them by the application of above mentioned HNO_3 oxidation method. It is expected, that the resulting layer would include Si nanocrystals surrounded by a SiO_2 shell.

2.3.2 Ge nanocrystals

In the case of Ge nanocrystal formation, Si wafers covered with SiO_2 or Si_3N_4/SiO_2 layers were loaded into an oil free evaporation chamber (Varian VT-460), and the system was evacuated down to 1×10^{-8} Torr. Ge ingot of 99.999% purity was supported on a molybdenum plate, and it was evaporated using an electron gun, at an evaporation rate of 0.01-0.03 nm/s, at a pressure of 1×10^{-7} Torr. During evaporation, and for an additional 1 minute after this process, the substrate temperature was kept at 350°C. The temperatures were monitored by small-heat-capacity Ni-NiCr thermocouples, while the film thicknesses were measured by a vibrating quartz probe.

Two series of samples were prepared depending on the thickness of bottom oxide layer. For initial experiments, Si substrates with 100 nm thick thermal silicon dioxide were prepared and the Ge was evaporated with different duration on the top of this structure. The second series of samples were prepared directly for memory purposes. It contained two types of thin chemical oxides and the two thinnest Ge nanocrystal layers based on the initial experiments.

As for the initial experiments, Ge nanocrystals were thermally evaporated with different evaporation times. Four different sets of samples were formed with 2, 4, 6 and 8 equivalent monolayers of Ge. During evaporation, the evaporated mass of Ge was monitored with vibrating quartz. (The term equivalent monolayer means the mass of a fully compact Ge layer.) After Ge evaporation, a part of the samples were covered with thick SiO_2 for XTEM measurements, and referred below as Samples No. 1', 2', 3', and 4', respectively.

In the case of thin film growth from vapor phase three basic modes of the growth process may occur, depending on the principal interactions between atoms of the substrate and atoms of the deposit [2−2]. These are: (a) layer by layer growth (Frank-van der Merwe type [2−3,2−4]), (b) island growth (Volmer-Weber type [2−5]), and Stransky-Krastanov [2−6,2−7,2−8] growth, at which one or several complete monolayers are formed before NC growth.

In the case of SiO_2 covered Si wafers studied in this work the top of the substrate is amorphous, so the Stransky-Krastanov type growth of Ge is excluded. The cohesion between germanium atoms is larger, than their adhesion towards silicon dioxide. Consequently, island growth (Volmer-Weber type) occurs. No wetting layer can be expected, which means that the Ge dots (under a certain density) may be independent from each other. Their shape is determined by the surface tension of Ge, that results in distorted spherical type rather than dome like islands.

2.4 Preparation of the metallization

All samples characterized by memory measurements underwent an appropriate chemical treatment [2−9] followed by metallization with Al evaporation on both sides. Samples with Si_3N_4 layers underwent an additional silicon nitride etch procedure on backsides, preceding the chemical treatment. The mentioned chemical treatment is as follows.

First, the samples were immersed into 1:1 solution of $H_2SO_4 + H_2O_2$ for 30 mins. This was followed by 1:20 solution of $HF + H_2O$ for 1 min and another 1:1 $H_2SO_4 + H_2O_2$ for 15 mins. Note, that the first and the last step forms a thin chemical oxide on the backside of the substrate, while the middle step removes it.

Finally, capacitors with 0.8 x 0.8 mm lateral sizes were formed by Al evaporation on both sides, and photolithography and Al-etching on the front side. The thickness of the Al layer was 1 µm in all cases. No post-annealing process was performed.

The two contacts during measurements are either on one of the capacitor squares on the top of the sample, and the other is at the bottom.

2.5 Annealing in forming gas

Annealing in forming gas (95% N_2 + 5% H_2) was performed on selected samples at 1000^OC for 1 or 3 hours.

2.6 Design considerations and summary of prepared samples

My main goals in the Ph.D. work were as follows:

– to prepare Si and Ge nanocrystals arranged in a sheet;

– to embed the nanocrystals into dielectric thin layers;

– to investigate the physical properties of the nanocrystals (such as their size, density and lateral separation), as well as their optical functions, as a function of deposition parameters;

– to prepare metal–insulator–silicon (MIS) structures with embedded nanocrystals and to investigate their charge storage properties primarily with memory window and retention measurements, as a function of nanocrystal properties, and the position of the sheet of nanocrystals inside the dielectric layer.

For accomplishing these goals, the following main ideas were considered for sample structures:

Planned goal:	Accomplished goal:
samples with uncovered nanocrystals on top of SiO_2/Si substrates	$\boxed{Ge}$ nanocrystals with different size on top of a SiO_2 covered Si substrate
samples with nanocrystals with different size, density and separation, embedded into different dielectric layers at different depths	$\boxed{Ge}$ nanocrystals with different size on top of a SiO_2 / Si, covered by another SiO_2 layer
	Si_3N_4/SiO_2/Si structures containing $\boxed{Ge}$ (with Si_3N_4 as the conver dielectric)
	$\boxed{Si}$ nanocrystals with different size and density on SiO_2/Si, SiN_x/Si and Si_3N_4/SiO_2/Si substrates, covered by SiO_2 or SiN_x
the study of the effect of annealing	$\boxed{Si}$ nanocrystals embedded in SiN_x covered Si substrates

Basic structural information of the studied samples is shown in *Table 2–1* and *2–2*. *Table 2–1* is dedicated to give a general idea of the prepared samples. Detailed description of the sample structures is shown in *Table 2–2*.

Table 2-1. Short description of the studied samples

Sample No.	Short description of the sample These samples were prepared to study…	Methods of structural investigations	Memory properties investigated?
N1	…the dependence of the composition of SiN_x single layers on top of Si, as a function of the ratio of input gases during LPCVD deposition.	ellipsometry	No.
N2			
N3			
SRX	…the role of annealing on the composition of the top and bottom SiN_x single layers, and on the crystallinity of the middle nanocrystalline Si layer.	ellipsometry, XTEM, XPS	No.
NI000	…the effect of LPCVD deposition time on the size and density of the forming *Si nanocrystals, embedded in Si_3N_4 layers, deep in the nitride*; …the memory properties as a function of nanocrystal properties, in the case of *MNS* structures.	ellipsometry, XTEM	Yes.
NI030			
NI045			
NI060			
NI120			
NI180			
NI300			
COA00	…the effect of LPCVD deposition time on the size, density and separation of the forming *Si nanocrystals, embedded at the Si_3N_4/SiO_2 interface*; …the memory properties as a function of nanocrystal properties, in the case of *MNOS* structures.	XTEM, XPS	Yes.
COA30			
COA60			
COA300			
G1	…the effect of evaporation time on the size, density and separation of the forming *Ge nanocrystals on top of SiO_2 layers*.	AFM, SEM, Van der Pauw	No.
G2			
G3			
G4			
G1'		XTEM	
G2'			
G3'			
G4'			
O000	…the memory properties as a function of nanocrystal properties, in the case of *MNOS structure with embedded Si and Ge nanocrystals in the nitride, close to the N/O interface*.	XTEM	Yes.
G025			
G050			
O060			
Q120			

Table 2–2. Basic structural information of the studied samples, with layer materials and layer thicknesses, as obtained by spectroscopic ellipsometry and cross-sectional transmission electron microscopy

Sample No.	Layer structure (layer materials and thicknesses – on top of the Si substrate)			
	Bottom layer	Middle layer(s)		Top layer
N1	SiN$_x$, 100 nm, (DCS to NH$_3$ ratio: 120/20)			
N2	SiN$_x$, 100 nm, (DCS to NH$_3$ ratio: 140/20)			
N3	SiN$_x$, 100 nm, (DCS to NH$_3$ ratio: 200/20)			
SRX	SiN$_x$, ~18 nm	Si NC, ~17 nm		SiN$_x$, ~18 nm
NI000	Si$_3$N$_4$, 40 nm			
NI030	Si$_3$N$_4$, 15 nm	Si NC, 2.2 nm		Si$_3$N$_4$, 32 nm
NI045	Si$_3$N$_4$, 15 nm	Si NC, ~3.9 nm		Si$_3$N$_4$, 32 nm
NI060	Si$_3$N$_4$, 15 nm	Si NC, 5.1 nm		Si$_3$N$_4$, 32 nm
NI120	Si$_3$N$_4$, 15 nm	Si NC, 8.4 nm		Si$_3$N$_4$, 32 nm
NI180	Si$_3$N$_4$, 15 nm	continuous nc-Si layer, ~15 nm		Si$_3$N$_4$, 32 nm
NI300	Si$_3$N$_4$, 15 nm	continuous nc-Si layer, ~23 nm		Si$_3$N$_4$, 32 nm
COA00	SiO$_2$, 2.5 nm	Si$_3$N$_4$, 40 nm		
COA30	SiO$_2$, 2.5 nm	Si NC (30 sec deposition time)		Si$_3$N$_4$, 40 nm
COA60	SiO$_2$, 2.5 nm	Si NC (60 sec deposition time)		Si$_3$N$_4$, 40 nm
COA300	SiO$_2$, 2.5 nm	Si NC (300 sec deposition time)		Si$_3$N$_4$, 40 nm
G1	SiO$_2$, 100 nm	Ge evaporated for ~25 sec		
G2	SiO$_2$, 100 nm	Ge evaporated for ~50 sec		
G3	SiO$_2$, 100 nm	Ge evaporated for ~75 sec		
G4	SiO$_2$, 100 nm	Ge evaporated for ~100 sec		
G1'	SiO$_2$, 100 nm	Ge evaporated for ~25 sec		SiO$_2$, 100 nm
G2'	SiO$_2$, 100 nm	Ge evaporated for ~50 sec		SiO$_2$, 100 nm
G3'	SiO$_2$, 100 nm	Ge evaporated for ~75 sec		SiO$_2$, 100 nm
G4'	SiO$_2$, 100 nm	Ge evaporated for ~100 sec		SiO$_2$, 100 nm
O000	SiO$_2$, 2.5 nm	Si$_3$N$_4$, 35 nm		
G025	SiO$_2$, 2.5 nm	Si$_3$N$_4$, 2.5–3 nm	Ge evaporated for ~25 sec	Si$_3$N$_4$, 35 nm
G050	SiO$_2$, 2.5 nm	Si$_3$N$_4$, 2.5–3 nm	Ge evaporated for ~50 sec	Si$_3$N$_4$, 35 nm
O060	SiO$_2$, 2.5 nm	Si$_3$N$_4$, 2.5–3 nm	Si NC, 5.1 nm	Si$_3$N$_4$, 35 nm
Q120	SiO$_2$, 2.5 nm	Si$_3$N$_4$, 2.5–3 nm	Si NC, 8.4 nm*	Si$_3$N$_4$, 35 nm

*The size of the NCs in this sample differs in horizontal and vertical direction.

2.7 Conclusions

Experimental procedures used in this work for different layer depositions and for the formation of Si and Ge nanocrystals were summarized. A complete list of the prepared samples is presented with their structural information.

Chapter 3 – Methods of investigation

3.1 Structural characterization

The thickness and composition of the Si_3N_4 and SiO_2 thin layers in the structures were determined by cross-sectional transmission electron microscopy (XTEM), energy-filtered cross-sectional transmission electron microscopy (EFTEM), X-ray photoelectron spectroscopy (XPS), and spectroscopic ellipsometry.

The size, distribution and composition of the nanoparticles were determined by cross-sectional transmission electron microscopy (XTEM), energy-filtered cross-sectional transmission electron microscopy (EFTEM), X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and scanning electron microscopy (SEM).

3.1.1 Transmission electron microscopy

Transparent samples for TEM were prepared by Ar ion milling. Images of the samples were taken in a Philips CM20 electron microscope operating at 200 keV and JEOL 3010 high resolution, 300 keV TEM, both measurements performed in MTA MFA. Characteristic nanocrystal sizes were determined based on all the visible nanocrystals observed in these cross-sectional transmission electron microscopy (XTEM) images.

3.1.2 Atomic force microscopy

The AFM was performed with a Veeco Nanoscope E STM/AFM instrument in tapping mode using Si_3N_4 tips with 20 nm radius and 0.06 N/m deflection spring constant in MTA MFA. The AFM measurements were performed on samples with Ge nanocrystals on SiO_2 covered Si substrates (on samples G1, G2, G3 and G4).

I define the surface coverage of NCs with the area occupied by Ge clusters divided by the total observed area. Practically, this value was obtained in AFM images with image processing. A threshold level value of 66.7% was applied for samples G1 and G2, and a value of 33.3% was applied for samples G3, and G4. The ratio of white and black pixels in these threshold images was assigned to the surface coverage. The threshold level value was lower for samples G3 and G4 than for samples G1 and G2 because of the increased surface roughness. As the average diameter of Ge NCs is known for each sample, one can obtain the surface density of NCs by dividing the area covered by NCs by the area of the disk corresponding to one individual NC. [BP−2]

3.1.3 Scanning electron microscopy

The SEM images of samples with Ge nanocrystals on SiO_2 covered Si substrates were taken by a LEO Gemini 1540 scanning electron microscope in MTA MFA.

3.1.4 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) measurements were carried out on electron spectrometer ESCALAB MK2 (VG) with Al K_α X-ray monochromatized source (hv = 1486.6 eV), performed by Surface Phenomena Researches Group (SPRG), Scientific Enterprise, Moscow.

The samples in initial state and after multistage Ar^+ ion etching (used for obtaining information from various depths) were investigated. The investigations were carried out in vacuum of 1×10^{-8} Pa. X-ray photoelectron spectroscopy was used as for investigations of phase composition, chemical state of atoms, and electronic structure of Si nanocrystals. The XPS spectra were recorded with speed of 0.1 eV/s with 100 scans. The spectrometer was adjusted using Ag reference. The charge effect was suppressed by charge neutralizer, the flood gun EMU-50. The beam of low energy electrons (30−45 eV) is suitable for neutralizing the charge of insulating samples during long XPS investigations. The physical/technical conditions for electronic spectra acquisition were selected in the best way to provide energy resolution of the spectrometer better than 0.6 eV.

3.1.5 Spectroscopic ellipsometry

Woollam M88 (1.63–4.43 eV), Woollam M2000 (1.24–5.04 eV) and Sopra ES-4G (1.5–5.0 eV) ellipsometers were used for the spectroscopic ellipsometry measurements. The measurements were performed in MTA MFA and at the University of Szeged.

The structural model used for modeling the samples with nanocrystals consisted of three layers on top of a silicon substrate. Only the middle layer in this model was considered to consist the nanocrystals. The dielectric function of this layer was modeled either by the effective medium approximation mixture of known dielectric functions or by parametric approximation. The former permitted to examine the composition of this layer, while the latter enabled to study the dependence of the dielectric function on the nanocrystal size.

Optical models for the silicon nitride layers

Effective medium approximation with Si₃N₄ and excess silicon

The Bruggeman Effective Medium Approximation (B−EMA) model can be used as the optical model of non-stoichiometric layers [BP−6,BP−9]. It mixes the dielectric function of two or three constituent materials by varying their volume fractions in an isotropic matrix. The requirement for B−EMA is that the sizes of the constituents are in the range or less than the wavelength of the measuring light, but large enough to preserve the bulk dielectric functions of the reference materials used in the B−EMA calculations.

This model can be applied to obtain the dielectric function of SiN_x layers, as well, by choosing stoichiometric Si_3N_4 [3−1] and silicon as the constituent materials [3−1,3−2,3−3]. However, the dielectric function of amorphous, polycrystalline, or crystalline Si are different, and consequently, different dielectric functions for the silicon component can be used. In our case, silicon is present in the amorphous form in the SiN_x layer, as obtained by cross-sectional transmission electron microscopy [BP−9], therefore the dielectric function of the amorphous silicon [3−4] should be used. The equation for the B−EMA that has to be solved to determine the volume fractions of the components and the complex dielectric function of the layer is

$$f_1 \cdot \frac{\varepsilon_1 - \varepsilon}{\varepsilon_1 + 2\varepsilon} + (1 - f_1) \cdot \frac{\varepsilon_2 - \varepsilon}{\varepsilon_2 + 2\varepsilon} = 0 \qquad\qquad (Eq.\ 3\!-\!1)$$

where f_1 *(unknown)* and ε_1 *(known)* are the volume fraction and the dielectric function of the first component, respectively, ε_2 *(known)* is the dielectric function of the second component, and ε *(unknown)* is the complex dielectric function of the effective medium film layer. The main advantages of this model are its simplicity and its ability to determine the N to Si ratio (stoichiometry) of a SiN_x film. However, the EMA is a mathematical model which do not consider the atomic densities, so the volume fraction of Si (which is the primary parameter obtained from the fit) must be corrected in order to determine the stoichiometry, according to the following equation:

$$x = \frac{(1 - f_1) \cdot 1.48 \cdot 4}{(1 - f_1) \cdot 1.48 \cdot 3 + f_1 \cdot 4.99} \qquad\qquad (Eq.\ 3\!-\!2)$$

where x is the stoichiometry of a SiN_x layer, f_1 is the volume fraction of silicon in the layer, in addition to the Si_3N_4 (that is the result of the fit), and the atomic densities for Si_3N_4 and Si were considered as $1.48 \cdot 10^{22}$ molecules/cm³ and $4.99 \cdot 10^{22}$ atoms/cm³, respectively [3−5].

Tauc-Lorentz model

The Tauc-Lorentz (TL) model is a parametric optical model. It considers one single direct band-to-band transition with its amplitude (A), broadening (C) and position (E_0). The energy gap (E_g) and a constant that corresponds to the contribution of transitions outside the measured spectral range, $\varepsilon_1(\infty)$ is also consisted in the model (see *Eq. 3–3*). The real part of the dielectric function is calculated by the Kramers-Kronig transformation of its imaginary part.

$$\varepsilon_2(E) = \begin{cases} \dfrac{A \cdot E \cdot E_0 \cdot C \cdot (E - E_g)^2}{(E^2 - E_0^2)^2 + C^2 \cdot E^2} \cdot \dfrac{1}{E}, & E > E_g \\ 0, & E < E_g \end{cases}$$

$$\varepsilon_1(E) = \varepsilon_1(\infty) + \frac{2}{\pi} \cdot \mathcal{P} \int_{E_g}^{\infty} \frac{\xi \cdot \varepsilon_2(\xi)}{\xi^2 - E^2} d\xi$$

(Eq. 3–3)

The obtained TL parameters for a low-pressure chemical vapor deposited stoichiometric Si_3N_4 layer were typically: $A = 151.5$, $E_n = 11.39$ eV, $C = 14$ eV, $E_g = 3.97$ eV, where the Mean Squared Error (MSE) of the fit was 0.85 [BP–3].

Optical model for the silicon dioxide layers

The dielectric function of the silicon dioxide layers in the optical model can be either taken from the literature [3–7], or obtained by a parametric model, such as the Cauchy model. The simplified non-absorbing Cauchy model is a slowly varying empirical function of the wavelength as can bee seen in the following equation:

$$n(\lambda) = \alpha + \frac{\beta}{\lambda^2}$$

(Eq. 3–4)

where $n(\lambda)$ is the real refractive index of the layer, α and β are the fit variables, and λ is the wavelength. The imaginary part of the refractive index is assumed to be zero.

Optical model for the silicon nanocrystal layers

The main question is the modeling of the silicon nanocrystal layer, because the dielectric function of Si depends on the size of the material, and this dependence is not well understood yet. There are several possibilities to model the dielectric function of Si NCs, for example:

(1) assuming that the dielectric function of the layer equals to the dielectric spectra of a known reference material,

(2) the Effective Medium Approximation (EMA) mixture of the known spectra of two (or more) materials,

(3) parametric modeling of the layer.

For option 1, I chose G. E. Jellison's fine-grained polycrystalline Si (fp-Si) [3–8] material which is based upon a CVD deposited thin-film silicon. As for option 2, I used single-crystalline Si (c-Si) [3–9], and amorphous Si (a-Si) [3–4] as the constituent materials for the Bruggeman EMA. I used S. Adachi's Model Dielectric Function (MDF) [3–6] for option 3. It is a complex model, but it gives a well-grounded physical background to the fitted values.

In the MDF the direct interband transitions (critical points – *CPs*) of Si are considered to describe the dielectric spectra. It considers three Damped Harmonic Oscillators (DHOs) at three different energies (E_0', E_1', E_2) with broadenings (γ_0', γ_1', γ_2, respectively) and strengths (C_0', C_1', C_2, respectively). Additionally, an excitonic transition with strength B_{1x} and a (2D)M_0 transition at E_1, both with broadening γ, and a (2D)M_2 transition, with strength F, and broadening γ at E_2 are considered.

In *Eq. 3–5*, these components of the dielectric spectra of nc-Si are shown (variable *E* is the photon energy in *eV*, and variable ε_x is the dielectric function of component *x*). The complex dielectric function of the nc-Si layer is considered as a sum of all contributions in *Table 3–1*:

$$\varepsilon_{nc-Si\ layer} = \varepsilon_1 + \varepsilon_2 + \varepsilon_3 + \varepsilon_4 + \varepsilon_5 + \varepsilon_6 + \varepsilon_\infty \qquad\qquad (Eq.\ 3–5)$$
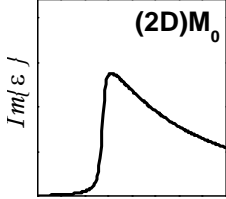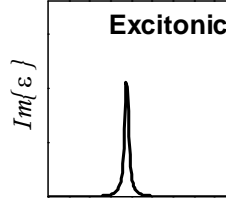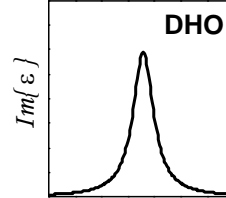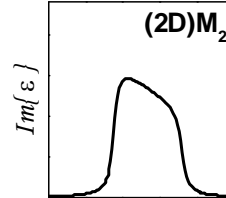
where ε_∞ is a constant corresponding to contributions from outside the measured photon energy range.

As an illustration, the MDF contributions to the imaginary part of the dielectric function of c-Si is shown in *Fig. 3–1 b*. This figure is a result of a simple fit procedure with the MDF model to the dielectric function of c-Si, taken from the literature [3–9]. *Fig. 3–1* a shows the imaginary part of the dielectric spectra of other reference materials taken from the literature. (The real part of the dielectric function is not shown, because the imaginary part alone illustrates the contributions well.)

For new materials, if there is no reference dielectric function data available, it is rather difficult to find the initial values of the parameters of MDF. However, if appropriate reference materials exist, this work becomes moderate. I chose a-Si, fp-Si, and c-Si as *reference materials* for the MDF (see the imaginary part of their dielectric spectra in *Fig. 3–1 a*), in order to explore the potential ranges of the parameters in the case of silicon.

In Ref. [3–10] it is stated, that amorphous (a-Si) and crystalline Si (c-Si) can be studied on a common basis, the MDF. The peaks corresponding to the critical points of c-Si are broadened in the case of the amorphous state. It is claimed that this effect can be explained by symmetry considerations, and it is due to the absence of the long-range order in the amorphous state [3–10]. However, in the case of a nanocrystalline material, the long-range order of the lattice harms similarly to the case of the amorphous silicon. Consequently, the broadening of the peaks corresponding to the CPs of c-Si is expected in the case of the nc-Si as well. These considerations open up the possibility to study the size effect by spectroscopic ellipsometry with MDF using carefully chosen initial parameters.

Table 3−1. Components of Adachi's Model Dielectric Function (MDF) [3−6]: equations for the dielectric function of the component, symbol of the photon energy of the peak of the component, symbol of the broadening of the component, and the shape of the imaginary part of the component

| Name	Equation for the complex dielectric function contribution	Symbol of the photon energy of the peak	Symbol of the broadening	Shape of the imaginary part
		…of the component transition		
(2D)M$_0$ transition	$\chi_1 = \dfrac{E + i \cdot \gamma}{E_1}$ $\varepsilon_1 = -1 \cdot B_1 \cdot \chi_1^{-2} \cdot \log\left(1 - \chi_1^2\right)$	E_1	γ	(2D)M$_0$
Excitonic transitions	$\varepsilon_2 = \dfrac{B_{1x}}{E_1 - E - i \cdot \gamma}$	E_1	γ	Excitonic
DHO at E_1'	$\chi_1' = \dfrac{E}{E_1'}$ $\varepsilon_3 = \dfrac{C_1'}{(1 - \chi_1'^2) - i \cdot \chi_1' \cdot \gamma_1'}$	E_1'	γ_1'	
DHO at E_0'	$\chi_0' = \dfrac{E}{E_0'}$ $\varepsilon_4 = \dfrac{C_0'}{(1 - \chi_0'^2) - i \cdot \chi_0' \cdot \gamma_0'}$	E_0'	γ_0'	DHO
DHO at E_2	$\chi_2 = \dfrac{E}{E_2}$ $\varepsilon_5 = \dfrac{C_2}{(1 - \chi_2^2) - i \cdot \chi_2 \cdot \gamma_2}$	E_2	γ_2	
(2D)M$_2$	$\chi_{2m} = \dfrac{E + i \cdot \gamma}{E_2}$ $\chi_{cl} = \dfrac{E + i \cdot \gamma}{E_{cl}}$ $\varepsilon_6 = -1 \cdot F \cdot \chi_{2m}^{-2} \cdot \log\left(\dfrac{1 - \chi_{cl}^2}{1 - \chi_{2m}^2}\right)$	E_2	γ	(2D)M$_2$
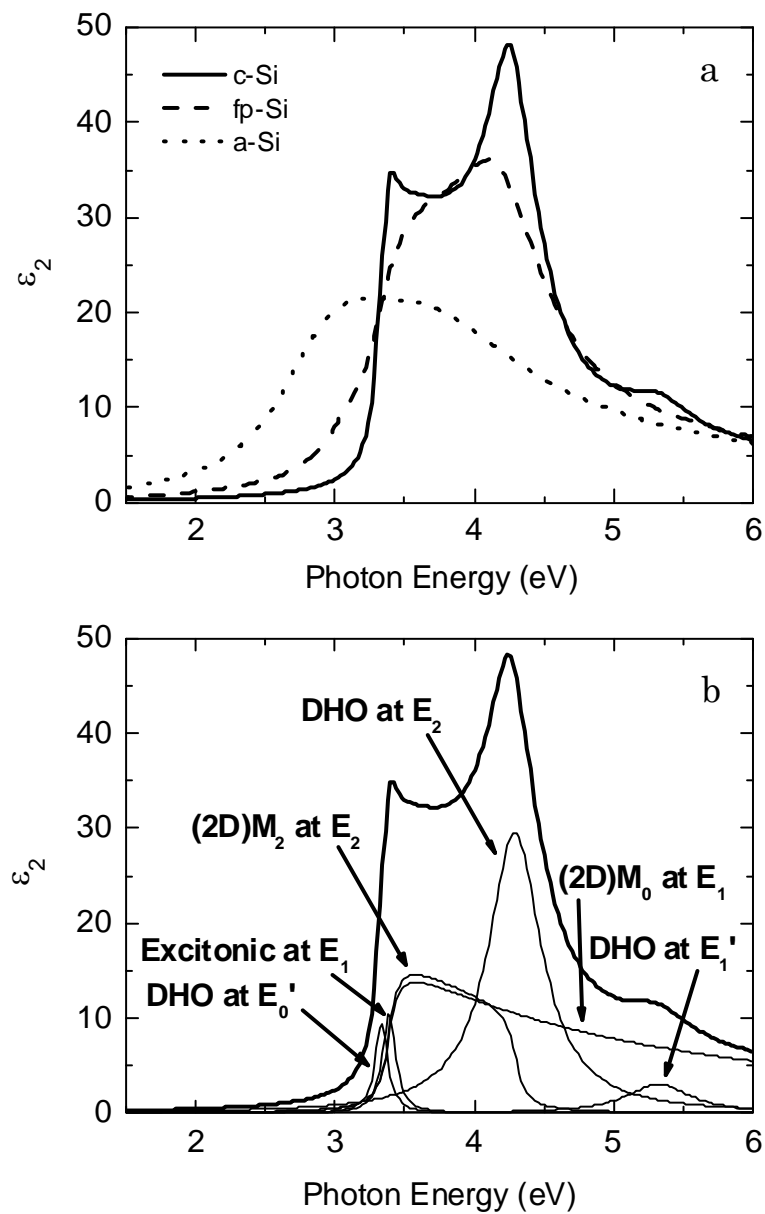
Fig. 3‒1. The imaginary part of dielectric spectra of the c-Si [3‒9], fp-Si [3‒8] and a-Si [3‒4] reference (a), and the results of the fit for the contributions for c-Si derived from the MDF model (b)

3.2 Electrical characterization

In this section, a brief summary is presented about the applied electrical characterization methods.

3.2.1 Van der Pauw measurements

The sheet resistance of selected samples were determined with a high-impedance system (insulating sample holder, Keithley 616 electrometer) after forming ohmic contacts using Sn dots alloyed by current impulse, and then preparing pre-contacts by rubbing Ga+In eutectics into the surface. The square-shaped samples were contacted at four corners for these measurements.

3.2.2 Capacitance-voltage hysteresis measurement

The capacitance-voltage (C−V) hysteresis curve was measured with a *HP4271B LCR meter*. The capacitance measurement was executed with a high-frequency (1 MHz) and low level (20 mV rms) signal. The DC bias voltage was supported by the external *Keithley 230 programmable voltage source*. The instruments were controlled by a software written in Pascal running on a PC with FreeDOS, via GPIB digital measurement control interface. A schematic of the cross section of the sample during electrical measurements is shown in *Fig. 3−2*.
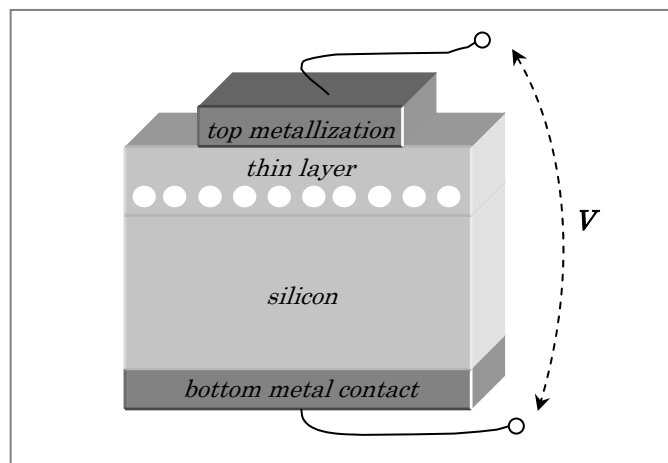
Fig. 3−2. A schematic cross-section of the sample during C−V hysteresis measurement

During C−V hysteresis measurement, DC voltage is applied across the sample, with gradually increasing value, until it reaches its limit. Then, the voltage is decreased, and changed until the opposite limit, and finally, it is decreased again towards the other limit. Simultaneous capacitance measurements are taken at every voltage value, yielding a C−V hysteresis curve. A typical C−V hysteresis curve is shown in *Fig. 3−3*, with circles

indicating the flat-band conditions (in this case, the flat-band capacitance is near 600 pF). Practically, the flat-band voltage is the DC voltage that has to be applied to the sample, to measure the flat-band capacitance.
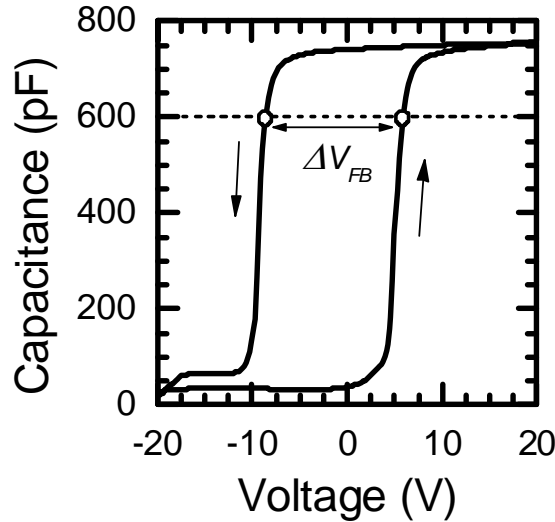

Fig. 3–3. A typical C–V hysteresis curve, with circles indicating the flat-band conditions

The width of the obtained hysteresis then represents the charge storage capability of the layer. The total injected charge can be calculated using the following equation:

$$Q = C_1 \cdot \Delta V_{FB}$$ *(Eq. 3–6)*

where C_1 is the maximum capacitance of the MIS element normalized to an area of unity, and ΔV_{FB} is the obtained flat-band voltage change in the hysteresis.

The time delay that occurs between the application of voltage and the beginning of the capacitance measurement can be crucial from the viewpoint of charge storage capabilities, because charging processes of the layer are exponentially dependent on time. The time that is required for our instrument (HP4271B LCR meter) to measure the capacitance is however, limited down to 130 ms.

3.2.3 Memory window measurement

Practically, during a memory window measurement, the flat-band voltage of the structure is determined after the charging voltage pulse. In fact, the method for this determination is not often reported in the literature. However, a fast analog method is well described in Ref. [3–11].

As a matter of fact, during memory measurements, a fast *digital* method was used in our case, that is described in the following. First, the capacitance of the sample was measured with the HP4271B LCR meter, at an initial voltage. This initial voltage is the first guess for the flat-band voltage. Based on earlier C–V hysteresis measurements, the

shape of the C−V curve had been already known, and so it became possible to calculate a second *suggestion* for the flat-band voltage. Technically, one measurement based on a single guess is often insufficient for reliable flat-band voltage determination, so further capacitance measurements are needed, always based on the previous result for the flat-band voltage. Within a few measurements, strong convergence is reached, and the flat-band voltage is determined with accuracy of 0.01 V.

3.2.4 Retention measurement

The other important memory property of a memory structure is the retention, which describes the charge storage ability of a device. Practically, the sample is charged (or discharged) by a writing (or erasing) voltage pulse, and the charge state of the layer is monitored continuously, as a function of time. The extrapolated memory window width for 1 and 10 years qualifies the sample.

During retention measurements, the electronic state of the sample between flat-band determinations (during waiting) is also not exactly described neither in the literature, nor among patents. If the sample is short-circuited during waiting, the injected charge starts to leak across the short-circuit, and the stored charge begins to decrease. A solution for retarding this current could be an insertion of a large resistance (such as an opened reed relay) into the circuit. However, it can not be considered as a complete separation of the top and bottom metallization of the sample, since most widespread reed relays have insulating resistance in the range of 10^{10} Ω, which is comparable to the typical resistance corresponding to the thin insulator layer of the sample itself, as obtained by high-sensitivity current-voltage measurements [BP−9]. As for our retention measurements, a HAMLIN HE721A0500 reed relay was used.

3.3 Conclusions

The methods of structural and electrical investigations were summarized in this chapter. Optical models for the spectroscopic ellipsometric evaluations were introduced. The evaluation of the atomic force microscope images in order to extract information about nanocrystal size, density and coverage was explained. The method for the capacitance−voltage hysteresis measurement was explained. A new method for the flat-band voltage determination was suggested which enabled the execution of memory window measurements. This new method was first suggested here, by the author himself. The measurement method of the retention was explained. The uncertainty of the flat-band voltage determination with the new method was estimated to be around 10^{-2} V.

Chapter 4 – Results of the structural investigations

4.1 SiN$_x$ single layers

Short description of the examined samples "N1, N2, and N3"

For our initial experiments with silicon nitride, SiN$_x$ single layers were grown on top of Si substrates by LPCVD. The thickness of the layers were kept at 100 nm and the SiH$_2$Cl$_2$ (dichloro silane – DCS) to NH$_3$ ratio was varied from 120 / 20 sccm, to 200 / 20 sccm in three steps by varying the gas flow speed of DCS (yielding samples N1, N2 and N3 in *Table 2–1*).

4.1.1 Spectroscopic ellipsometric study

The stoichiometry of these films was determined by spectroscopic ellipsometry. The optical models that were used for this examination were the Bruggeman Effective Medium Approximation (B-EMA) and the Tauc-Lorentz model.

First, the B-EMA model was applied. The Si to N ratio is shown in *Fig. 4–1* as a function of DCS to NH$_3$ gas flow ratio.
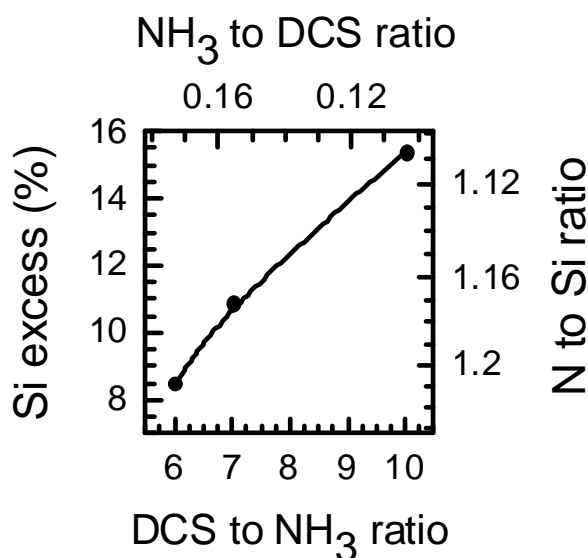
Fig. 4–1. The composition of the SiN$_x$ layers obtained by ellipsometry, characterized by the N to Si ratio and the Si excess %, as a function of the adjusted dichloro silane (DCS) to NH$_3$ ratio

However, it is possible to study the layer properties with a more robust, parametric ellipsometric model, namely, the Tauc-Lorentz model. In *Fig. 4–2*, the obtained energy gap

and refractive index calculated for 623.8 nm is shown for different DCS to NH_3 ratios in the case of layers with 100 nm thickness (the same samples as in the previous study above). It is apparent that with increased DCS flow the refractive index increases towards the silicon refractive index of 3.6 and simultaneously, the band-gap energy decreases towards the silicon band-gap energy of ~1.1 eV. It is important to note, that similar results have been found by French et al. [4−1] – however, they examined NH_3/DCS gas flow ratios above 0.2 and they used deposition temperature of 850^OC which is 20^OC higher than in our case.

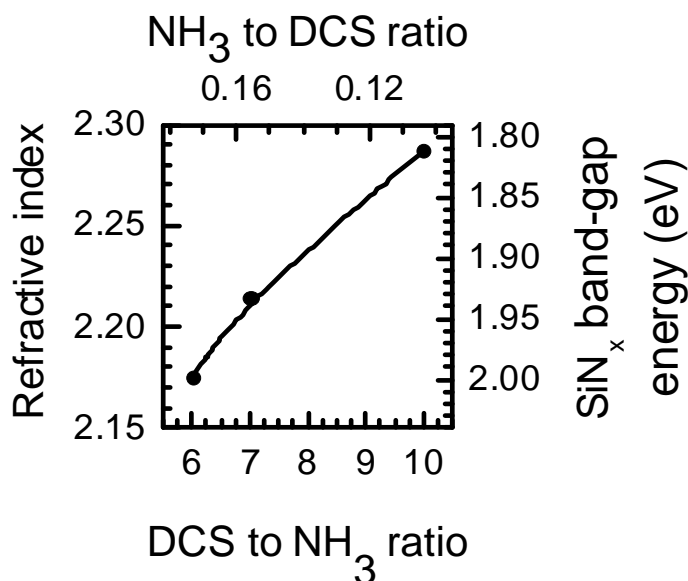*Fig. 4−2. The refractive index calculated for 632.8 nm of the SiN_x layers and the SiN_x band-gap energy obtained by ellipsometry, as a function of the adjusted dichloro silane (DCS) to NH_3 ratio. (The connection between the two different scales of the vertical axes is approximated.)*

4.2 Si nanocrystals between SiN_x layers

Short description of the examined sample "SRX"

Multilayer structure was deposited by LPCVD at 810^OC and 30 Pa using SiH_2Cl_2 and NH_3 in three steps. During the deposition, the flow rate for the top and bottom layer was 100/25 sccm, and for the middle layer it was 100/0 sccm (SiH_2Cl_2/NH_3, respectively). The first and the last step was the deposition of a non-stoichiometric nitride. The middle step yielded a nanocrystalline Si layer. The duration for all deposition steps was 5 min, respectively. The sample was then annealed for 1 and 3 hours at 1000^OC in forming gas.

4.2.1 Spectroscopic ellipsometric study

For modeling the non-stoichiometric nitrides and the nc-Si layer, the Bruggeman effective medium approximation (EMA) model was applied. According to cross-sectional transmission electron microscopy (XTEM) results there are crystalline phases in the middle layer [BP−7]. Based on the deposition parameters and the XTEM results I state that the middle layer is a nanocrystalline silicon layer. Previous results [BP−6] show that when considering the crystalline phase in a nanocrystalline silicon layer, beside a long-range ordered crystalline silicon material, a short-range ordered (fine-grained) crystalline silicon material has also to be considered with another dielectric function for the EMA model. Therefore, in the EMA model for the middle layer a crystalline (c-Si) [3−9], an amorphous (a-Si) [3−4], and a fine-grained polycrystalline (fp-Si) silicon [3−8] component material were included.

The results of ellipsometric evaluation on an as-deposited sample is shown in *Table 4−1*. The obtained thickness of all three layers were nearly identical, namely around 17−18 nm. Unexpectedly, the top SiN_x layer contained significantly less excess Si than the bottom layer. It has been found that the dielectric function of the middle layer is determinatively described by the fp-Si material.

Table 4−1. Fitted layer thickness and composition (in the top and bottom layers: percentage of a-Si excess; in the middle layer: percentage of fp-Si + a-Si + c-Si, respectively), and the mean-squared error (MSE) for the fit for the as-deposited and the annealed samples

	As-deposited	Annealed for 1 hour	Annealed for 3 hours
Top SiN_x layer thickness (nm)	18.2±0.1	13.9±0.1	13.5±0.1
Top SiN_x layer composition (a-Si %)	6.5±0.2	4.5±0.2	3.8±1
Middle nc-Si layer thickness (nm)	17.2±0.2	17.6±0.1	17.4±0.1
Middle nc-Si layer composition (fp-Si + a-Si + c-Si %)	86±2 + 4.1±0.5 + 9.9±1	77.7±1.6 + 2.2±0.4 + 20.1±1	77.3±1.2 + 2.8±0.3 + 19.9±1
Bottom SiN_x layer thickness (nm)	18.6±0.4	18.8±0.3	19.4±0.4
Bottom SiN_x layer composition (a-Si %)	17.3±3.1	17±2.3	19.5±1.5
MSE	11.25	6.59	9.98

As an effect of annealing (see *Table 4−1*), the results suggest that the top nitride layer becomes thinner and poorer in Si. It can be interpreted by a fast diffusion of Si atoms through the grain boundaries of the nc-Si layer. While the thickness and composition of the bottom layer remains the same within errors, the outgoing silicon from the top layer may remain in the nc-Si layer. There is a significant change in the composition of the middle layer. The lower nc-Si to c-Si ratio means that the amount of the crystalline phase

increases, which is consistent with the increase of the long-range order and the increase of the grain size.

If an extra SiO_2 layer is taken into account on the top of the structures, the mean-squared error (MSE) of the fit decreases for all cases. It is experienced that omitting the top oxide layer or omitting the nc-Si component from the middle layer causes an increased difference between the measured and fitted curves. Nevertheless, the presence of the top oxide layer was confirmed by X-ray photoelectron spectroscopy.

The deviation for Ψ is most significant in the UV range of the spectrum containing the direct interband transition energies of 3.4 and 4.3 eV (365 and 289 nm, respectively) of Si. Due to the increased absorption at these resonance energies, the penetration depth is smallest just in this most sensitive part of the spectrum. This is the reason of the slightly increased error (confidence limits denoted by "±" in *Table 4−1*) of the constituent ratios of the bottom layer compared to that of the top layer.

4.2.2 Transmission electron microscopy study

The as-deposited and one of the annealed samples described in the previous section were studied by cross-sectional transmission electron microscopy (XTEM). It has been found that the middle layer contained nanocrystalline silicon grains with sizes between 5 and 10 nm [BP−6]. After annealing performed at 1000^OC for 1 hour smaller number of randomly oriented grains were found [BP−6].

4.2.3 X-ray photoelectron spectroscopy study

X-ray photoelectron spectroscopy (XPS) study did not show any increase of crystallinity in the middle layer due to annealing. However, it has been found that the Si content (Si_a + Si-nc) increases from 11 % to 31 % in the bottom SiN_x layer. The Si content of the top SiN_x layer is uncertain due to the increased amount of SiO_2 in this layer according to XPS (see *Fig. 4−3*). [BP−10,BP−11]
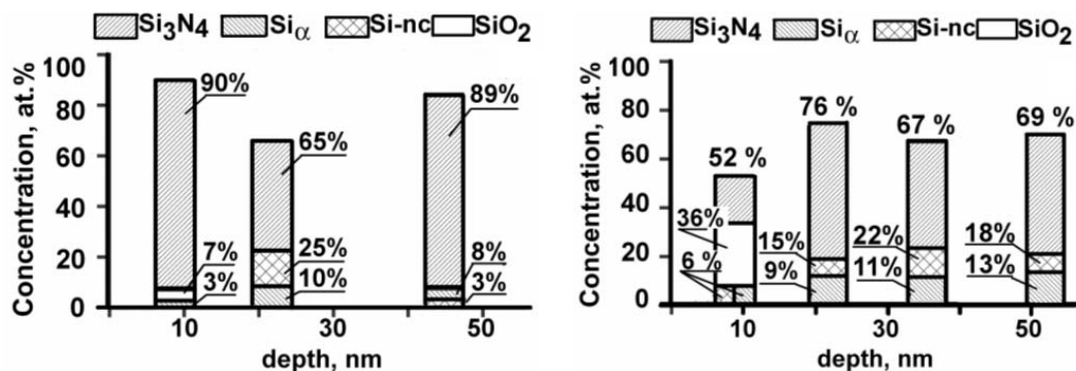
Fig. 4−3. XPS results for as-deposited (left) and 1 hour, 1000^OC annealed sample (right) with $SiN_x/nc-Si/SiN_x$ multilayer on top of Si substrate, respectively [1]

[1] The XPS measurements were carried out by D. L. Wainstein and A. I. Kovalev, Surface Phenomena Researches Group (SPRG), Scientific Enterprise, Moscow

4.3 Si nanocrystals between Si₃N₄ layers

*Short description of the examined samples "NI300, NI180, and NI120"*

Films containing nanocrystalline Si (nc-Si) layers were deposited by LPCVD in three steps, where the flow rates of the two input gases were varied during the deposition. Both the top and bottom layers were deposited as stoichiometric silicon nitride layers according to section 2.2. For the middle layer (that contained Si nanocrystals) procedure described in section 2.3 was applied.

Five different sets of structures were prepared on Si wafers depending on the deposition time for the middle layer. Three of them were examined by spectroscopic ellipsometry in-depth: with deposition times for the middle layer of 5, 3, and 2 mins – sample NI300, NI180, and NI120, respectively.

It was expected, that shorter deposition times for the middle layer correspond to thinner layers, and hence, smaller NC sizes. Moreover, it was expected that below a certain duration of deposition the resulting NC layer becomes incontinuous and one obtains NCs embedded into the surrounding dielectric.

4.3.1 Transmission electron microscopy study

Cross-sectional transmission electron microscopy (XTEM) shows evidence that there are crystalline Si grains in the middle layer, and the thickness of this layer decreases with decreasing deposition times (see *Figs. 4–4 a–c* for 5, 3 and 2 mins of deposition times for middle layer, respectively). Thickness values extracted from XTEM images confirm those obtained by spectroscopic ellipsometry.
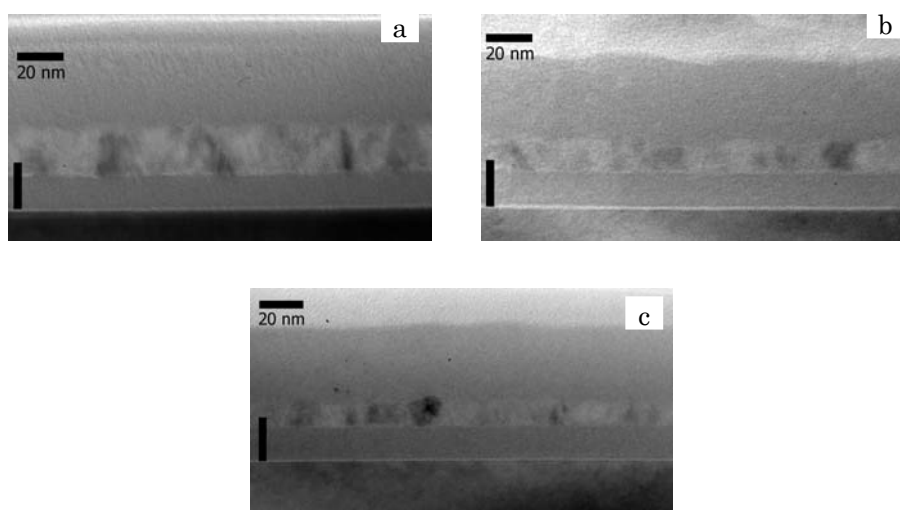
Fig. 4–4. High-resolution cross-sectional transmission electron microscope images of samples NI300 (a), NI180 (b) and NI120 (c)

An important result was obtained by high-resolution XTEM, namely, that the middle Si nanocrystal layer is incontinuous below deposition times of 60 sec and continuous above 120 sec. However, deposition time of 120 sec results in a layer with large Si grains almost separated from each other by Si_3N_4 bridges, but electrical characterization showed that these grains are electrically connected to each other.

As for samples with deposition time of 60 sec or shorter, high resolution XTEM revealed obviously separated Si nanocrystals. Cross-sectional nitrogen map of these samples (see *Fig. 4−5*) reveal "nitrogen bridges" between Si nanocrystals (NCs). Note, that here white dots represent Si_3N_4 material in the layer – and black dots any other material. These images prove that Si NCs are separated from each other and moreover, opens the possibility to approximate the average interdistance between NCs. These values are 4.3 nm, 4.0 nm, and 5.9 nm for samples NI120, NI060, and NI030, respectively. It is important to note, that there are separating nitrogen bridges in the case of NI120 as well, that could be the explanation for anomaly in ellipsometric results compared to thicker, i.e. continuous Si NC layers.

Average Si NC sizes for these samples obtained from dark field XTEM images (see *Fig. 4−6*) are shown in *Fig. 4−7*. Based on the average interdistance between the NCs and the obtained NC sizes, the lateral density of the NCs is approximated to be in the order of $\sim 10^{12}\,cm^{-2}$.

The logarithmic dependence of the NC size as a function of the deposition time suggests the saturation of the NC size with increasing deposition time (as shown in *Fig. 4−7*). As a matter of fact, the increasing deposition time means increasing the total Si amount in the growth process. This is in contradiction with the observed decrease of the NC growth rate. Consequently, the increase of the NC density must be responsible for the increasing amount of Si in the growth process. It means the increased probability of surface diffusion of Si on the surface. *Fig. 4−6* confirms this theory, namely: increasing NC density is seen with increasing the deposition time (from sample NI030 to sample NI120).
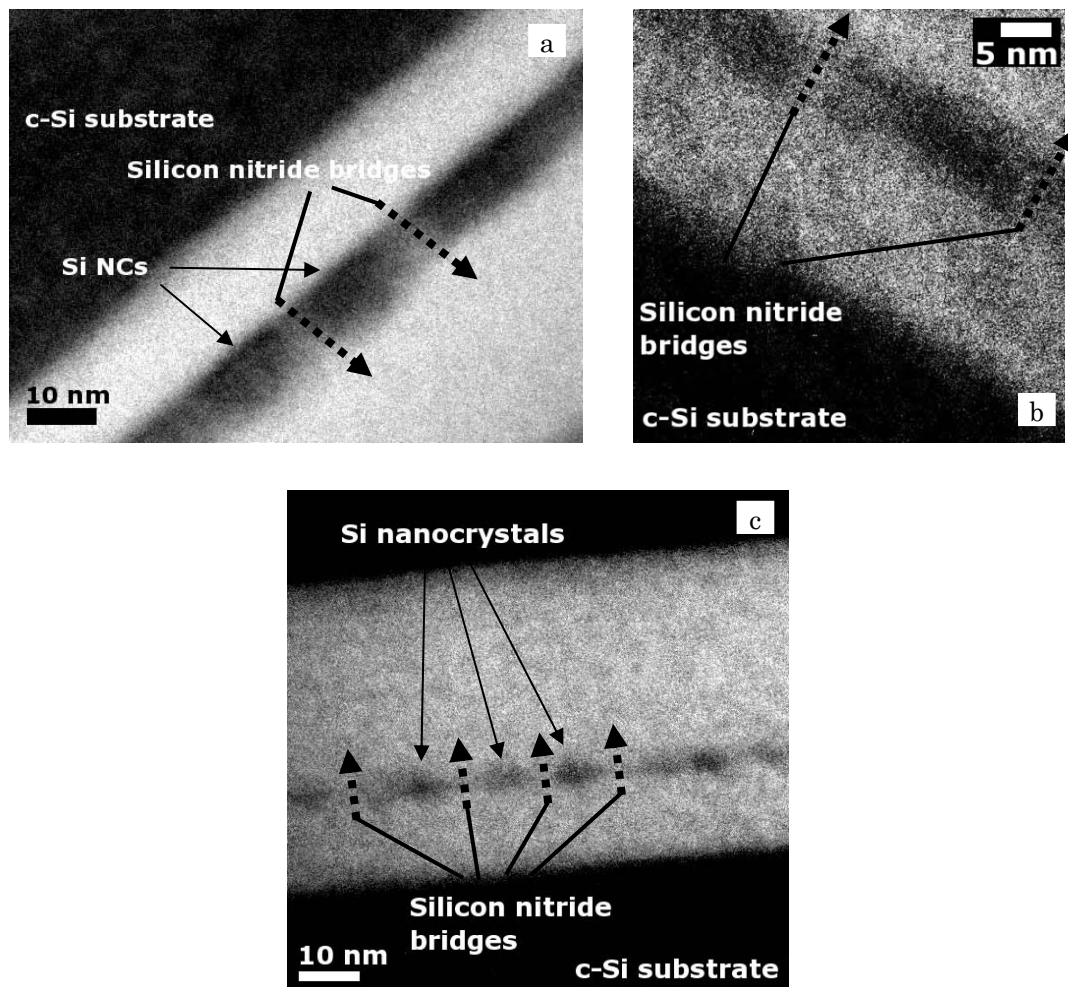
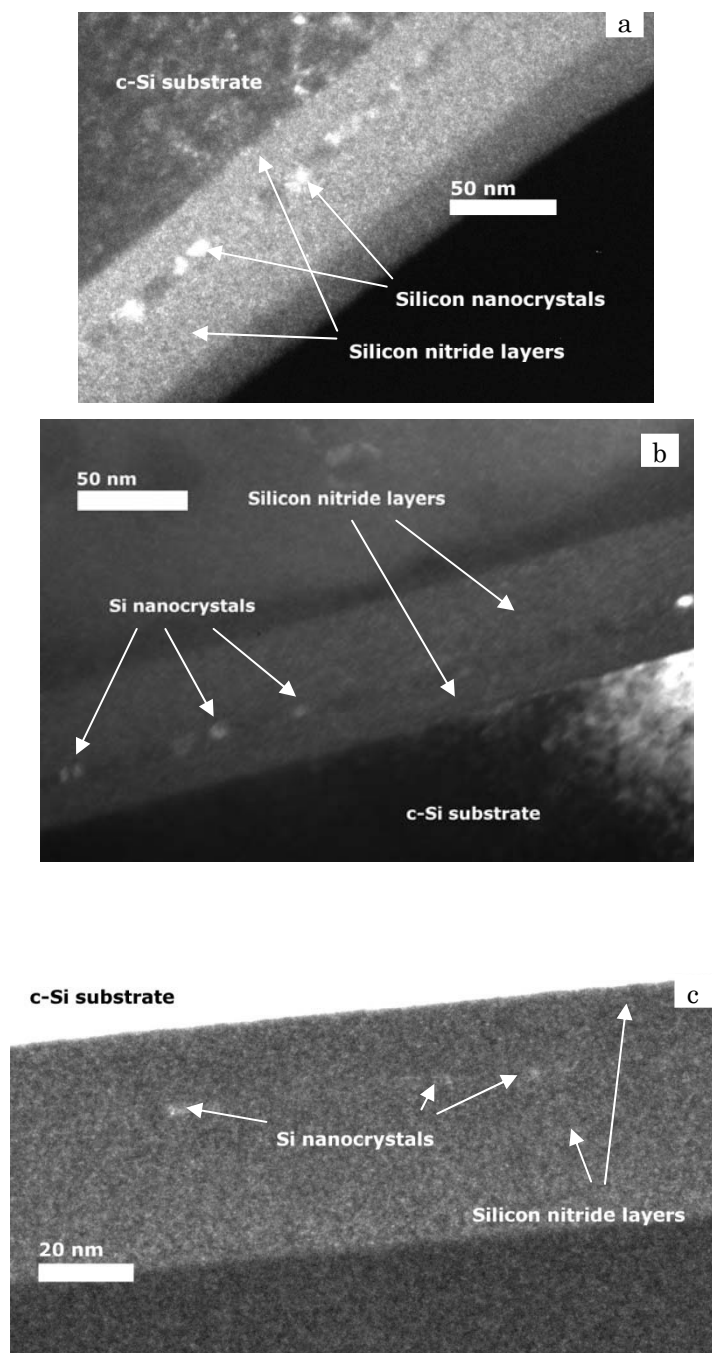*Fig. 4−5. Energy-filtered high-resolution XTEM image of sample NI120 (a), NI060 (b), and NI030 (c)*
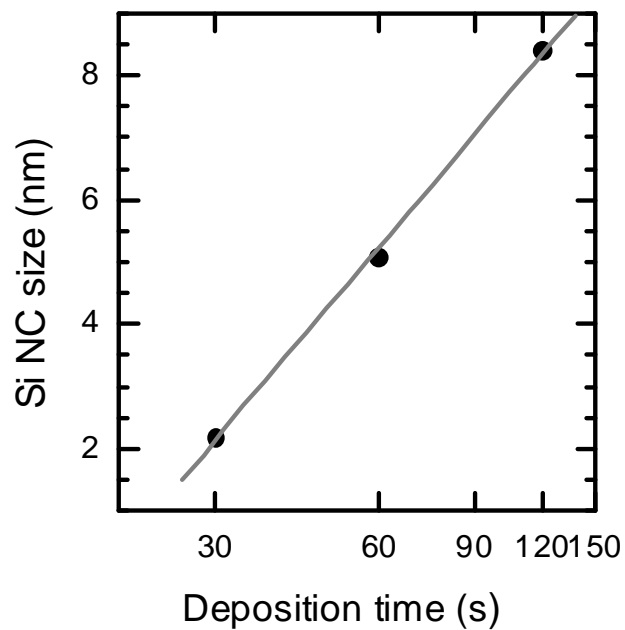
Fig. 4–6. Dark field cross-sectional transmission electron microscope image of samples NI120, NI060, and NI030 (a, b, and c, respectively)

Fig. 4−7. Si NC size obtained in dark-field XTEM images as a function of deposition time (for samples NI120, NI060 and NI030)

High resolution bright field zero loss XTEM images are shown in *Fig. 4–8*. The ordered structure inside the Si nanocrystals is visible, confirming their crystalline structure.
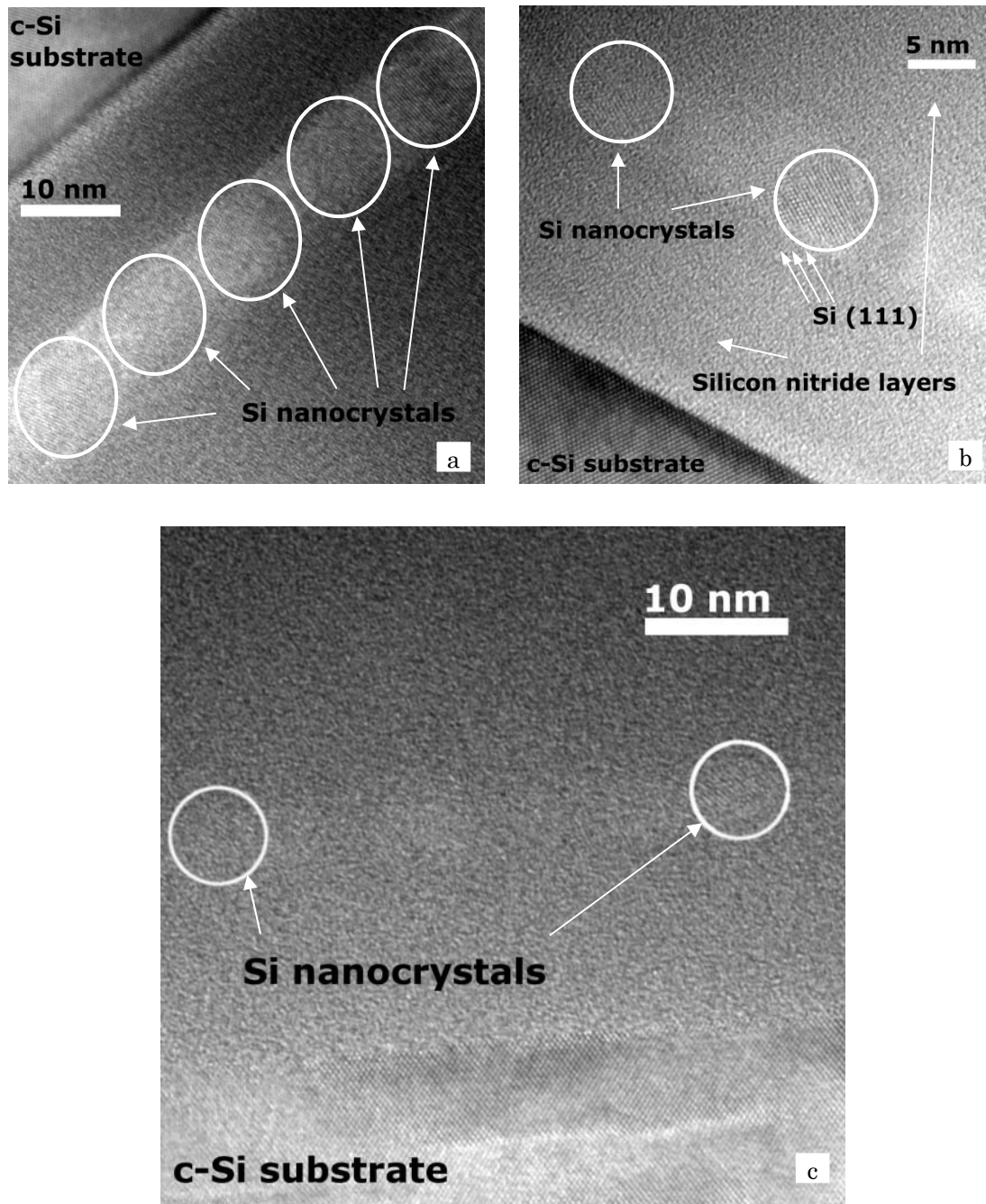
Fig. 4–8. High-resolution XTEM image of sample NI120 (a), NI060 (b), and NI030 (c)

4.3.2 Spectroscopic ellipsometric study

As for the three different optical models for the middle layer mentioned in section 3.1 *(optical model for the silicon nanocrystal layer)*, a comparison is presented between them in terms of the MSE of the fit for the studied samples in *Table 4–2*. It is seen, that the fit quality improves by using MDF. The two measured ellipsometric angles, Ψ and Δ (dots), and the fitted values (solid lines) are plotted in *Fig. 4–9* in the case of sample NI300. It is seen in the figure, that in the case of using the fixed fp-Si as the dielectric function for the middle layer, the fitted Ψ and Δ deviates more from the measured ones than in the case of the MDF parametrization of the layer.
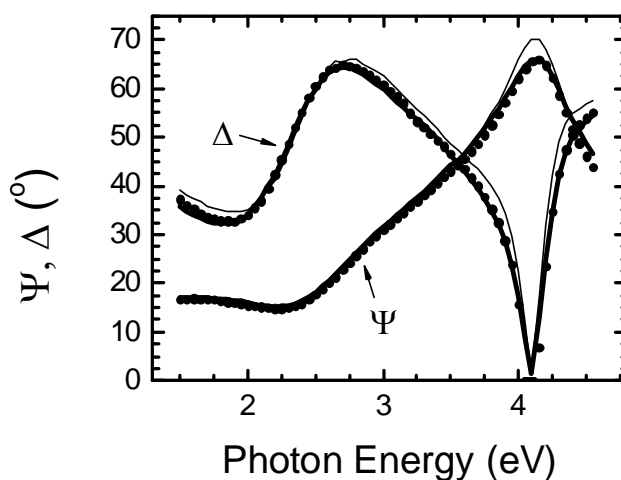
Fig. 4–9. Measured (dots) and fitted Ψ and Δ in the case of sample NI300 (thin line: fit using the dielectric spectra of fp-Si for the middle layer; thick line: fit using MDF parametrization of the middle layer)

Fitting procedure was performed on single-crystalline Si (c-Si) [3–8], fine-grained polycrystalline Si (fp-Si) [3–7], and amorphous Si (a-Si) [3–4] with dielectric functions taken from the literature to bracket the parameters of MDF to established limits (see *Table 4–3*). It is seen that the CP features depend strongly on the crystallization of the material. Similar work can be found in the literature for N-implanted c-Si [4–2]. Note, that as for the a-Si and fp-Si reference, the DHO at E_1' (around 5.33 eV) was not taken into account during the fit, because of their relatively small contribution.

Table 4−2. MSE of fits using different models for the middle layer

Model for the middle layer ▶	fp-Si	EMA (a-Si + c-Si)	MDF using fp-Si as a basis for initial parameters
sample NI300	3.07	2.39	1.30
sample NI180	1.99	2.33	1.14
sample NI120	3.52	4.05	1.83

During the fit for the studied samples, the layer thicknesses, the strength and broadening parameter of the DHO at E_2 (C_2 and γ_2, respectively), and γ, as the broadening parameter of all CPs at E_1 were fitted only. The other parameters were fixed at the obtained MDF values for the fp-Si reference. It means, that the fp-Si reference was used as a basis during the fit (thus, during the construction of the dielectric function of the middle layer). Note, that the thickness of the bottom layer and γ_0' was fixed for sample NI180 and NI120 at the fitted value of sample NI300.

It has been found that the optical thickness of the middle layer is decreasing systematically with decreasing deposition time. The selected MDF parameters (C_2, γ_2, γ) also changed systematically from sample to sample (see *Table 4−4*). It is seen that the DHO contribution at E_2 (C_2) to the imaginary part of the dielectric function of the middle layer is decreasing with decreasing deposition time. Additionally, the broadening of all critical points at E_1 (γ) is increasing with decreasing the thickness of the middle layer (*Table 4−4*). It is important to note, that γ and C_2 follow similar tendencies fitted on the reference materials in the direction of the amorphous state (*Table 4−3*). [BP−3]

Table 4−3. Obtained MDF parameters for the c-Si [3−8], fp-Si [3−7], and a-Si [3−4] reference materials

	Fitted value for...		
	c-Si	fp-Si	a-Si
E_1	3.39±0.03	3.31±0.01	2.85±0.06
B_1	5.52±0.52	6.30±0.10	7.98±0.34
B_{1x}	0.60±0.57	-	-
γ	0.06±0.02	0.17±0.01	0.33±0.09
E_2	4.30±0.01	4.24±0.01	3.91±0.18
C_2	3.20±0.19	3.19±0.15	2.09±0.98
γ_2	0.11±0.01	0.19±0.01	0.38±0.05
F	3.68±0.26	3.89±0.26	0.99±1.38
E_0'	3.33±0.04	3.09±0.04	2.54±0.07
C_0'	0.31±0.49	0.35±0.14	1.32±0.65
γ_0'	0.03±0.02	0.13±0.03	0.28±0.04
E_1'	5.33±0.08	–	–
C_1'	0.33±0.14	–	–
γ_1'	0.11±0.05	–	–
MSE	0.34	0.32	0.34

It is seen in *Table 4–4*, that the fitted C_2 and γ_2 parameters for sample NI120 are quite decreased with respect to sample NI300 and NI180. It indicates structural changes in the nanocrystalline layer that result in the invalidity of the used ellipsometric model (note that the MSE is significantly higher). Practically it means that either the used model is not adequate or there are not enough measured points to satisfy the fit. As a matter of fact, this structural change is successfully revealed as the discontinuity of the Si NC layer at deposition times of 120 sec or shorter (see the study of these samples by XTEM in the previous section).

Table 4–4. The obtained top, middle, and bottom layer thicknesses, and the fitted MDF parameters of the middle layer as a function of the deposition time for the middle layer. In the case of sample NI180 and NI120, d_{bottom} and γ_0' are fixed at fitted values of sample NI300

	Parameter	Values for...		
		sample NI300	sample NI180	sample NI120
Deposition parameter	Deposition time for the middle layer (sec)	300	180	120
Layer thickness	d_{top} (nm)	32.6±0.2	33.4±0.1	30.6±0.1
	d_{middle} (nm)	23.3±0.9	15.2±0.3	11.5±0.2
	d_{bottom} (nm)	15.2±0.8	*fixed (15.2)*	*fixed (15.2)*
MDF parameters	C_2	2.39±0.24	2.32±0.13	0.11±0.03
	γ_2	0.21±0.01	0.25±0.01	0.04±0.01
	γ	0.26±0.04	0.32±0.01	0.39±0.01
	γ_0'	0.23±0.06	*fixed (0.23)*	*fixed (0.23)*
	MSE	1.30	1.14	1.83

The dielectric functions of a-Si and fp-Si, and the obtained dielectric spectra of the middle nc-Si layer are plotted in the *Figs. 4–10 a, b*. Looking at the figures, the systematic change of the dielectric function of the silicon is obvious as a function of deposition time (i.e. nanocrystal size). Note, that similar dependence has been found in the case of Ge nanocrystals embedded in SiO_2 layers, recently, by our group [BP–4,BP–5]. The decrease of the amplitudes suggests the presence of more amount of dielectric (or void) inside the nc-Si layer (or less amount of semiconductor material).
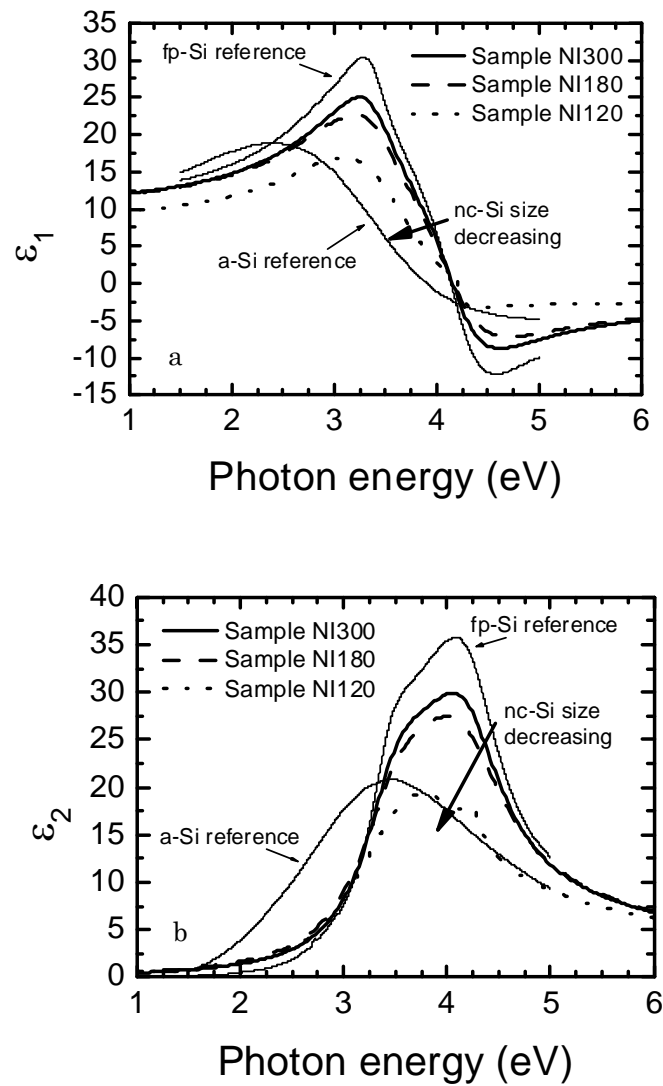
Fig. 4–10. The real (a) and imaginary part (b) of the dielectric spectra of the middle nc-Si layer for the studied samples and the dielectric spectra of reference materials (a-Si and fp-Si)

4.4 Comparison of results obtained on samples with Si nanocrystals between SiN$_x$ and Si$_3$N$_4$ layers

The preparation of Sample NI300 included a deposition step with duration of 5 mins, with DCS gas flow rate of 100 sccm, on top of Si$_3$N$_4$. This resulted in a nanocrystalline Si layer with 23.3 nm thickness. In section 4.2, the same deposition time and gas flow rate of DCS was applied but on top of Si-rich silicon nitride. The thickness of the resulting layer in that case was 17.2 nm only. It is apparent that the ~6 nm difference between these thickness does not come from ellipsometric inaccuracy, but from a physical effect which is suggested to be the different nucleation mechanism of Si on *Si-rich* and on *stoichiometric* silicon nitrides. Moreover, in the case of samples with Si nanocrystals between SiN$_x$ layers, there was an unexpected difference in the Si content of the top and bottom SiN$_x$ layers as well, i.e., the bottom layer contained much more excess Si.

Based on this comparison, it can be assumed that during Si deposition on Si-rich silicon nitride, a part of the Si diffuses into the underlying SiN$_x$ layer. This assumed process could explain both the difference between nanocrystalline Si layer thicknesses and the difference between the Si content of top and bottom SiN$_x$ layers.

4.5 Si nanocrystals between Si$_3$N$_4$ and SiO$_2$ layers

Short description of the examined samples "COA300, COA60 and COA30"

Thin SiO$_2$ layers prepared by HNO$_3$ oxidation [4−3] on top of Si substrates were subsequently inserted into the LPCVD tube and Si NC deposition, which has been described in previous chapters, was executed with varying deposition time. This was followed by a subsequent Si$_3$N$_4$ layer deposition.

It was expected that Si NC formation took place during introduction of DCS onto the SiO$_2$ layer, similarly than in the case of Si NC formation on top of Si$_3$N$_4$ layers. However, it is apparent that in present case, different deposition times needed to obtain continuous and/or discontinuous Si NC layers than for the case of Si NC deposition onto Si$_3$N$_4$ due to the different surface structure of SiO$_2$ and Si$_3$N$_4$.

4.5.1 Transmission electron microscopy study

Fig. 4−11 shows the XTEM image of sample COA300, which consisted of a thin SiO$_2$ tunneling layer, a thick Si NC layer deposited by LPCVD with duration of 5 min, and a thick Si$_3$N$_4$ capping layer. The Si NC layer is continuous and present in all areas of the film. Incontinuous Si NCs were detected in the case of sample COA30 by XTEM, as shown in Fig. *4−12*. The size of the particles is estimated to be around 15 nm, but they are not present in all areas of the film. (Fig. *4−13* shows another are of sample COA30, without the NCs.) It was obtained also by XTEM that the thickness of the thin SiO$_2$ layer on top of the Si substrate is around 2.5 nm.

Different nucleation mechanism of the Si NCs is suggested for this structure than for the structure with Si deposition on silicon nitride (which was discussed in section 4.2 and 4.3). Based on the similar NC layer thickness observed in samples COA300 and COA30 (see *Figs. 4−11* and *4−12*), a *critical thickness* of the continuous nc-Si layer (around 20 nm, in this case) is suggested, with incubation time between below 30 sec. Similar critical thickness was obtained in Ref. [4−4] for the formation of thin polycrystalline Si layers with CVD. The deposition time increase after 30 sec is then followed by the formation of further Si NCs with sizes around this critical thickness (~20 nm), until a continuous layer was formed (as seen in *Fig. 4−11*). In summary, with increasing the deposition time, the mean size of the Si NCs remains at a critical level (around 20 nm in this case), but with increasing density. This process operates until a continuous layer is formed due to coalescence. Further increase of the deposition time leads to the increase of the thickness of this layer. This is in correspondence with the model published in Ref. [4−5] by Stoker et al., who investigated CVD Si NC growth on SiO_2, and found that the NC mean size experiences a rapid growth at the initial stage of the deposition, which is followed by only a slight change of size with time.
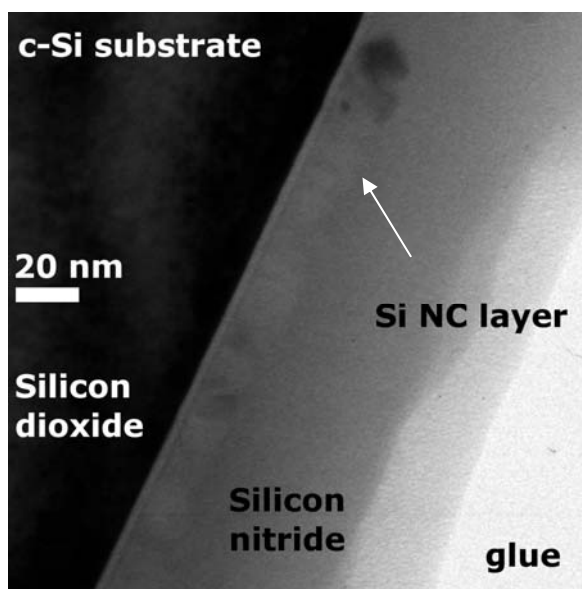
Fig. 4−11. XTEM image of sample COA300
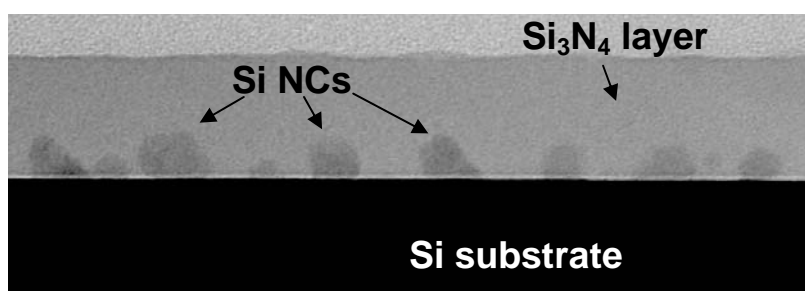
Fig. 4−12. XTEM image of sample COA30 showing presence of Si NCs
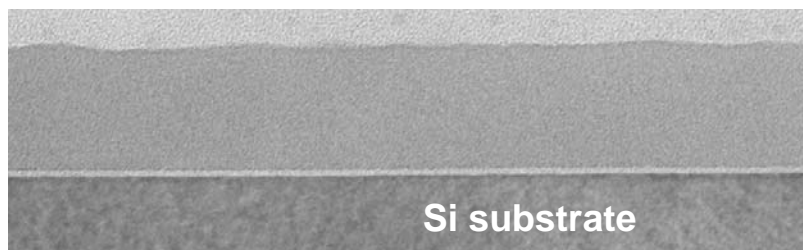
46

Fig. 4–13. XTEM image of sample COA30 showing lack of Si NCs

4.5.2 X-ray photoelectron spectroscopy study

XPS showed indication of Si NC existence at the interface of SiO_2 and Si_3N_4, in the case of samples COA30 and COA60. *Fig. 4–14* provides fine structure of the Si 2s line of sample COA60 at the interface of Si_3N_4 and SiO_2 layers. After deconvolution and fitting the main components, the Si-Si, Si-N, and Si-O bonds were identified. [BP–10,BP–11]

The Si 2s spectra were consistently decomposed into the three Gaussian components: one is at 154–155 eV which correspond to Si-O bonds in SiO_2, the other at 152.8–153 eV corresponds to $Si_{3-x}N_{4+x}$, and the third at 151-151.5 eV relates to Si-Si bonds in Si nanocrystals. The phase composition can be quantitatively calculated from the integrated area of the respective Gaussian peak divided by the total area of the spectral line. Quantities of these components vary a little with depth into interface region. The increasing of SiO_2 intensity is naturally accompanied by decreasing of Si NC concentration.

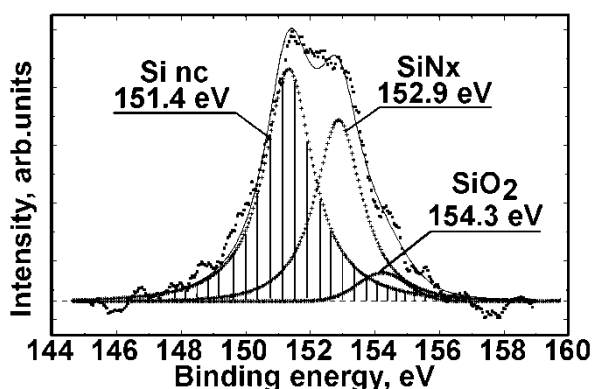*Fig. 4–14. Si 2s photoelectron spectrum of sample COA60
after Ar ion etching at depth of 38 nm* [1]

Fig. 4–15 shows the photoelectron spectra of sample COA30. Comparing the area of the Si NC components on *Figs. 4–14* and *4–15*, it can be seen that the concentration of Si nanocrystals at the interface of SiN_x/SiO_2 in sample COA30 is less than the one is in sample COA60.

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[1] The XPS measurements were carried out by D. L. Wainstein and A. I. Kovalev, Surface Phenomena Researches Group (SPRG), Scientific Enterprise, Moscow
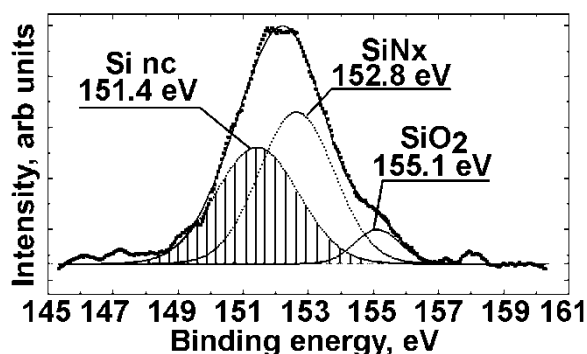
*Fig. 4−15. Si 2s photoelectron spectrum of sample COA30 after Ar ion etching at depth of 38 nm* [1]

4.6 Ge nanocrystals on top of SiO$_2$ layers

4.6.1 Transmission electron microscopy study

The obtained XTEM images of Ge NCs for the *first series of samples* (samples G1', G2', G3', and G4') are presented in *Fig. 4−16*. The first layer on the Si substrate is an approximately 100 nm thick amorphous SiO$_2$ layer with a homogeneous contrast, that is characteristic for the amorphous materials (see *Fig. 4−16*). Next to that a thin layer consisting of Ge nanocrystals (we refer to it as Ge NC layer) separates the top 80 nm thick region of SiO$_2$. The contrast in intensity of XTEM image for individual Ge dots indicates that they are crystalline, with different orientation.

It is also seen, that they are separated indicating the Volmer-Weber type of layer growth, as it was expected. The Ge NC layers exhibit increasing thickness with increasing evaporation time. The actual layer thickness values obtained from XTEM images are presented in *Table 4−6*. However, larger thickness was obtained for sample G1' than for sample G2'. There are two possible explanations for that fact. First could be, that deposition parameters were not kept sufficiently precisely in case of such ultrathin layers, while second is that TEM is a local method. The former is not reasonable because there is systematic difference between the samples obtained by electrical measurements. The latter is true, i.e. in other regions the thickness of the "layer" formed from Ge NCs might be larger.

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[1] The XPS measurements were carried out by D. L. Wainstein and A. I. Kovalev, Surface Phenomena Researches Group (SPRG), Scientific Enterprise, Moscow
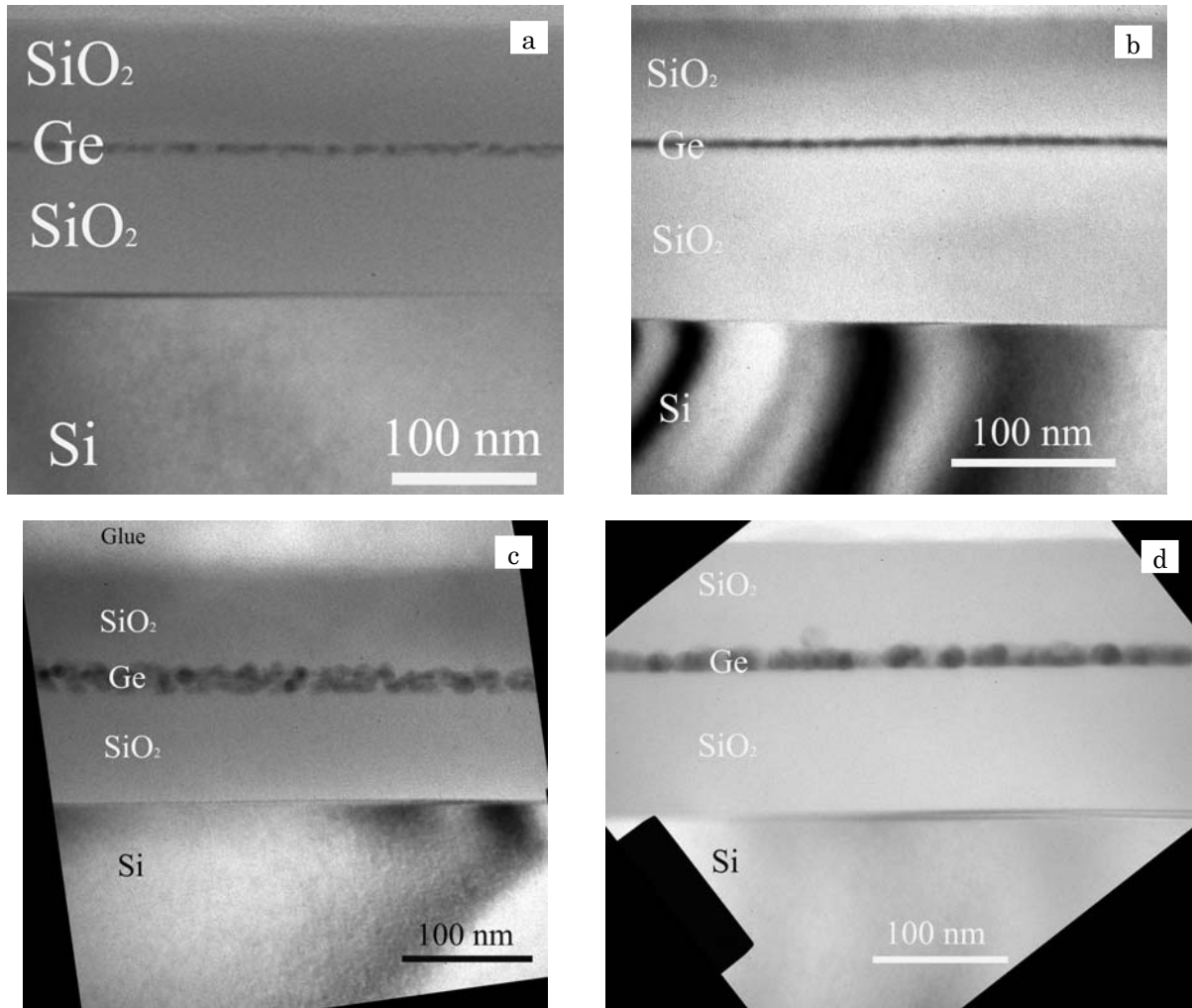
Fig. 4–16. Cross-sectional transmission electron microscopy image of samples G1', G2', G3', and G4' with SiO₂ capping layer (a–d, respectively).

It has been found for sample G3' that the Ge nanocrystals resettled in two rows, on top of each other, with an average size in vertical direction that is half of the layer thickness. For all the other samples, only one row of nanocrystals was found, with average size in vertical direction equal to the layer thickness. Again we arrived to the matter of inhomogeneity vs. TEM locally measured data. In the case of sample G3' other regions were observed as well, where NCs are situated in one row. Consequently, the two row configuration is not characteristic overall for sample G3'.

Table 4−6. The estimated evaporation time and Ge NC layer thickness obtained in XTEM images

Sample No.	Estimated evaporation time, s	XTEM Ge NC layer thickness, nm
G1'	25	9 ± 2
G2'	50	6 ± 1
G3'	75	18 ± 3
G4'	100	15 ± 2

Our further experiments were performed by considering this work as a basis. The two shortest evaporation times were chosen to initiate Ge NC formation with sizes 10 nm or smaller. Two different series of samples were formed depending on the capping layer, for which SiO_2 and Si_3N_4 layers were chosen.

XTEM measurements on *samples with SiO_2 capping layer* revealed existence of separated Ge nanocrystals on top of chemical oxide covered Si substrates. In *Fig. 4−17*, bright-field and dark-field XTEM images are shown obtained in the case of sample with Ge evaporation time of ~50 sec. Size of Ge NCs was obtained to be between 4 nm and 4.5 nm. Note, that in the case of Ge deposition onto thicker oxide with the same deposition time, 6 nm was obtained as the Ge NC size. This 2 nm different could indicate the error either for deposition accuracy or for thickness determination. Dark-field image show clearly that the Ge exist in nanocrystalline form in the layer. In *Fig. 4−18*, XTEM bright-field and dark-field images are shown of structures with Ge evaporation time of ~25 sec, respectively. In this case, Ge NC size of 4–6 nm was obtained.

As a matter of fact, no Ge NCs were observed by XTEM in the case of Si_3N_4 capping layer. This observation is in correspondence with the one published by Shklyaev et al. [1−11], namely: at high temperatures a part of the oxygen content of the SiO_2 departs from the layer as SiO and GeO (see section 1.3). Shklyaev et al. investigated temperature ranges of 600°C or lower, while in our case Si_3N_4 deposition takes place at 810°C which is much higher.
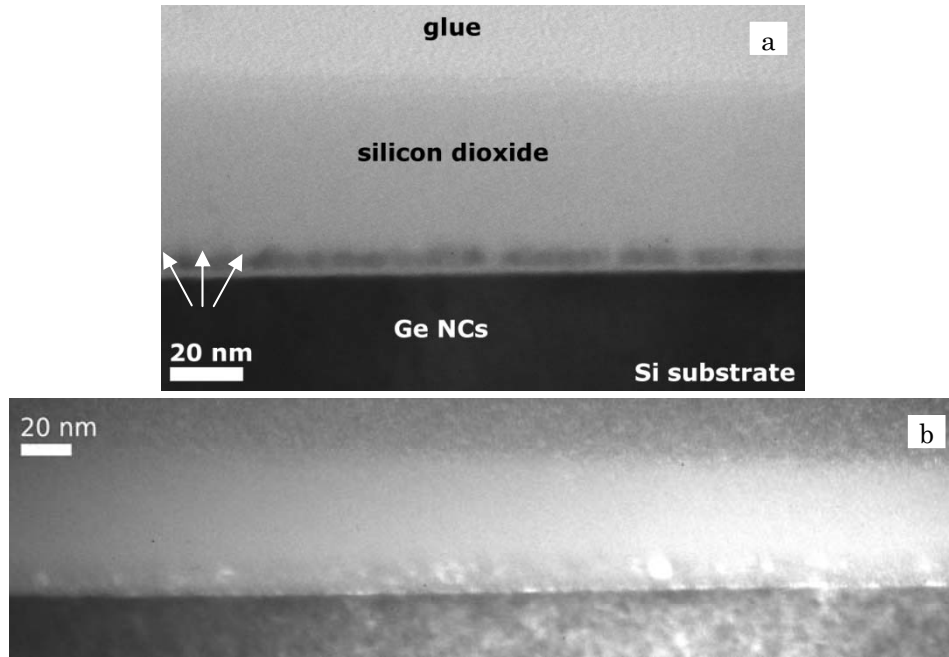
Fig. 4−17. Bright field (a) and dark-field (b) XTEM images of MOS structure containing Ge nanocrystals (with evaporation time of ~50 s)
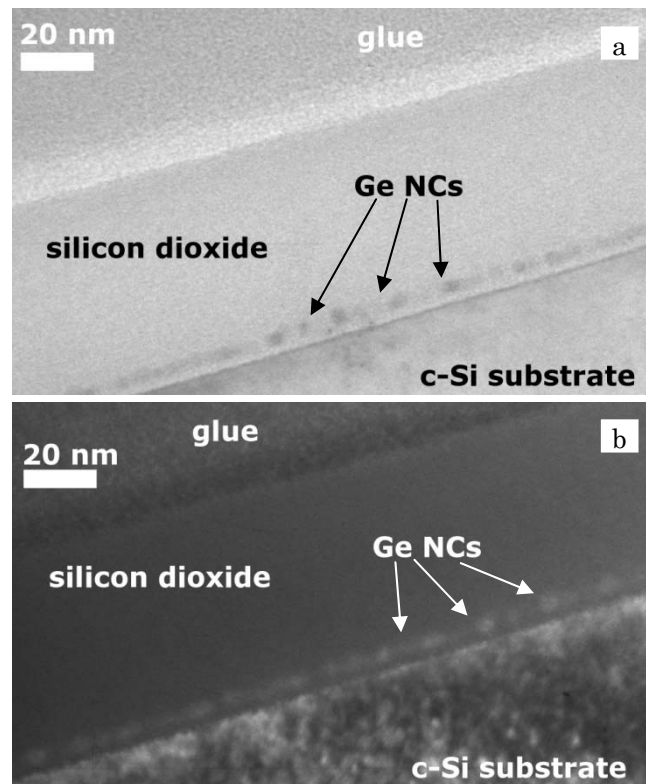

Fig. 4−18. Bright field (a) and dark-field (b) XTEM images of MOS structure containing Ge nanocrystals (with evaporation time of ~25 s)

4.6.2 Scanning electron microscopy study

No reliable SEM images were obtained for initial samples G1 and G2. The SEM images of samples with thicker Ge NC layer (samples G3 and G4) show well distinguished nanocrystals with 20.4±4.1 nm and 30.2±11.3 nm sizes, respectively (see *Fig. 4−19*). Note, that there is a strong coalescence mechanism taking place in case of sample G4 which results in an increased scatter of the NC sizes.

It has been found by SEM that the lateral nanocrystal size is larger than the vertical size observed in XTEM images in case of samples G3 and G4. The extracted lateral Ge NC size, the surface coverage and the surface density of Ge NCs is shown in *Table 4−7*. It has been found that the average NC size depended strongly on the evaporation time, with the exception of sample G2, the average diameter of NCs increased linearly with the evaporation time. However, as well as in NC sizes obtained in SEM images, there is an increased scatter of the size in the case of sample G4.
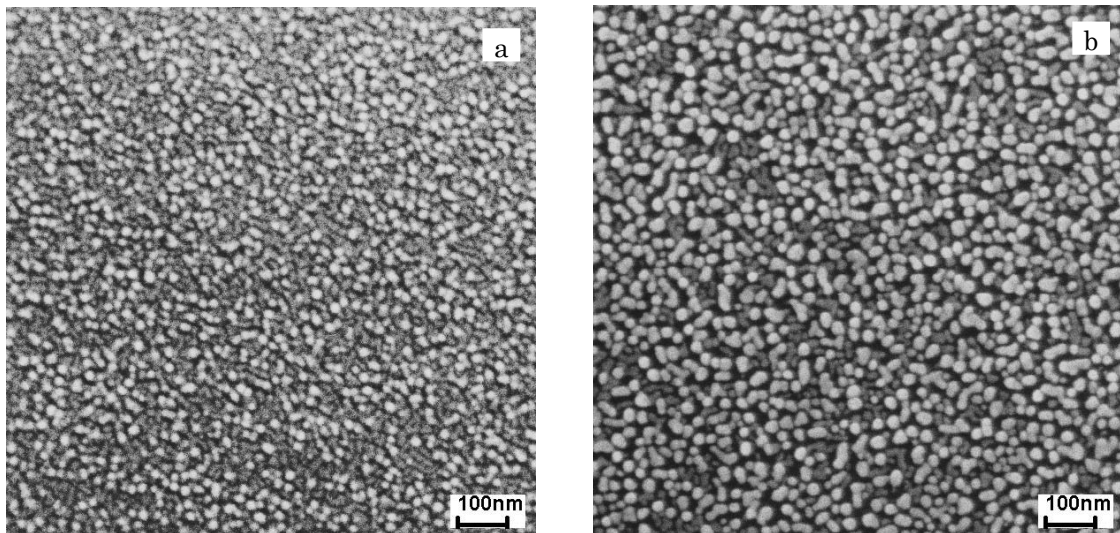
Fig. 4−19. Representative scanning electron microscopy images of samples G3 (a) and G4 (b) with image area of 1 µm × 1 µm

4.6.3 Atomic force microscopy study

AFM was performed on the first series of samples only, as there is a significant noise visible in the case of sample G1 and G2 in the first series. It suggests the limitations of AFM in the case of this type of samples.
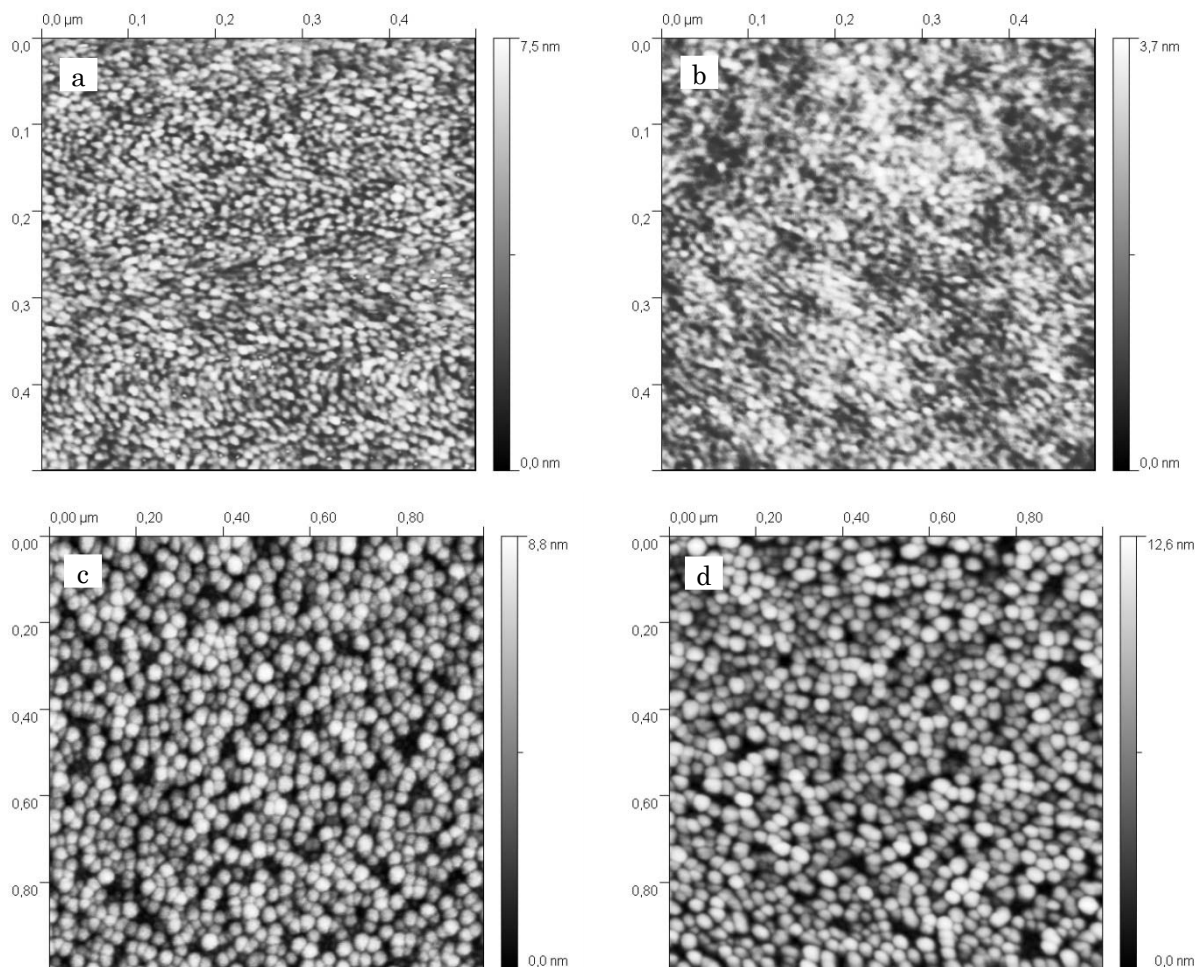
Fig. 4−20. Representative atomic force microscopy images of samples G1–G4 (a–d, respectively)

The obtained AFM images are shown in *Fig. 4−20*. The surface coverage is relatively large in all samples, and that's why there is strong correlation between the surface density of NCs and the square of the size of NCs (see *Table 4−7*). Note, that the obtained densities are practically between 10^{11} and 10^{12} $1/cm^2$, that is just the ideal case for the application in non-volatile memory structures [1−3]. The Ge NC sizes that were obtained by AFM are around double of the sizes obtained by XTEM. Nevertheless, this size difference is usual in literature [4−6], and is suggested to be caused by the finite AFM tip size.

Table 4−7. The average lateral nanocrystal diameter, the average distance between nanocrystals, the surface coverage of nanocrystals, and the surface density of nanocrystals (as obtained by AFM study)

Sample No.	Average lateral NC diameter, nm	Average distance between NCs, nm	Surface coverage of NCs, %	Surface density of NCs, NC/cm^2
1	8.9 ± 1.3	3.7	95.2	1.53×10^{12}
2	11.0 ± 2.0	5.5	97.8	1.03×10^{12}
3	29.6 ± 4.2	5.6	80.2	1.16×10^{11}
4	39.8 ± 9.8	2.1	89.5	7.20×10^{10}

The surface density of Ge NCs decreased with increasing evaporation time, and hence, increasing amount of Ge present on the surface. There is a sudden drop in the density between samples G2 and G3, that may indicate a change in the NC forming mechanism. Indeed, it is reported in the literature, that during the Volmer-Weber growth of evaporated Ge layers on SiO$_2$ covered Si substrates, the nanocrystal formation is divided into three stages [4−7]. First, adatoms adsorb on the surface of the substrate that create nucleation sites. After a finite time, as the second stage, the Ge islands are so extended that the probability of capturing by the top of an existing island is larger than forming new nucleation centers on the surface, for incoming new atoms. As a consequence, there is a stagnation of the surface density of NCs during this stage. Finally, during the third stage, the coalescence of NCs occurs, causing a sudden drop in their density. Note, that similar stages of the NC growth mechanism is suggested for Si nanocrystals on top of SiO$_2$ covered Si substrates [1−3].

The results suggest that the second stage of formation took place in the case of samples G1 and G2, because the change of the surface density of NCs is relatively small between them. As for sample G3, there is a sudden drop in the surface density of NCs indicating their coalescence, while in sample G4, a further coalescence occurred according to both AFM and SEM images.

4.6.4 Van der Pauw study

The electrical properties of the layers were characterized by sheet resistance measurements (see section 3.2 for the measurement details). The results of the measurements are shown in *Table 4−8*. It was obtained, that samples corresponding to shorter evaporation times, and hence, smaller NC sizes, have systematically higher sheet resistance. The relation between the sheet resistance and the average NC diameter can be expressed by a power law:

$$R_{sq} = 9.84 \cdot 10^4 \cdot d^{-3.25} \hspace{4cm} \textit{Eq. (4−1)}$$

where R_{sq} is in GΩ, and d is in nm. This dependence is presented in *Fig. 4−21* along with the experimental points. The correlation coefficient of the fit is 0.99.

Table 4−8. The estimated evaporation time, Ge NC layer thickness obtained from XTEM images, and the sheet resistance of Ge NC layers

Sample No.	Estimated evaporation time, s	XTEM Ge NC layer thickness, nm	Sheet resistance, GΩsq
G1	25	9 ± 2	96.0
G2	50	6 ± 1	29.7
G3	75	18 ± 3	2.36
G4	100	15 ± 2	0.467

Electrical conductance of separated metallic or semiconducting islands on top of insulator layers are widely studied from the 1960's [4−8,4−9,4−10,4−11,4−12], and the subject receives attention even nowadays [4−13,4−14]. The authors agree in a model where the lateral conductivity is determined by tunneling mechanism between islands (or nanocrystals), while the concentration of carriers taking part in the conduction is thermally activated. The activation energy is reciprocal function of the NC diameter. So, the conductivity – and so the resistivity – is an exponential function of the NC size. However, in our case, a power function was obtained between the sheet resistance and NC size.
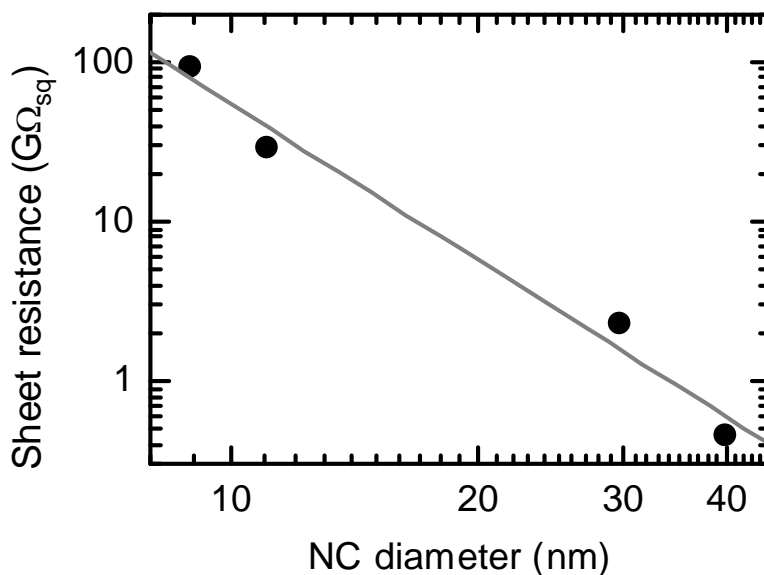

Fig. 4−21. Experimental (dots) and fitted by Eq. (4−1) (line) sheet resistance of the Ge NC layers as a function of the average NC diameter

4.7 Si and Ge nanocrystals on top of Si₃N₄/SiO₂ layers

This type of structure consisted of an additional Si_3N_4 layer between the SiO_2 layer and the nanocrystals. The nanocrystals were then covered with another Si_3N_4 layer. On one hand, the Si_3N_4 layer as a substrate for NC formation would play a favorable role during surface adhesion, and on the other hand, it was thought to protect Ge nanocrystals to react with the bottom SiO_2 layer during further high temperature steps (i.e. the LPCVD Si_3N_4 deposition). The schematics of the suggested structure is shown in *Fig. 4–22*.
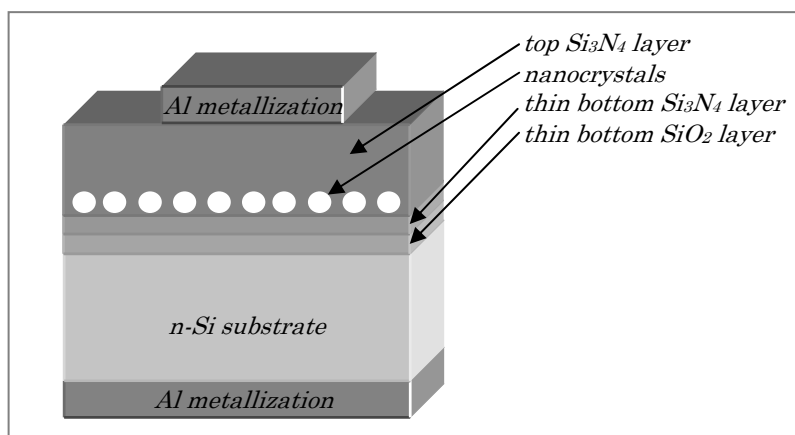
Fig. 4–22. Schematic cross-section of the suggested structure of metal-nitride-nitride-oxide-silicon (MNOS) samples with embedded Si or Ge nanocrystals, inside the nitride

Short description of the examined samples "O060, Q120, G025, and G050"

In the followings, the formation method and functional role of the thin layers in the structure illustrated above are described.

– The thin bottom SiO_2 layer on top of the Si substrate was prepared according to the procedure defined in section 2.2 [BP–8].

– The thin bottom Si_3N_4 layer was deposited by LPCVD at 810°C for 2.5 min. The thickness of this layer was obtained to be between 2.5–3 nm according to high-resolution XTEM images (see *Fig. 4–23*).

– As for the Si NC layer, two preparation methods were used. First, an LPCVD deposition time of 60 sec was used (being identical to NC deposition method for sample NI060). The physical properties of such NC layer is described in section 4.3. Sample exhibiting this kind of Si NC deposition were labeled as sample "O060".

– The second method involved an LPCVD deposition time of 120 sec (similar to NC deposition method for sample NI120). It was followed by a subsequent oxidation of the resulted continuous Si NC layer with HNO_3, with the same technique as described in section 2.2. Sample exhibiting this kind of Si NC formation method were labeled as sample "Q120".

– The planned Ge NC layer was evaporated under the same conditions as the two thinnest Ge NC layers formed during initial study of this method (see section 4.6). Samples exhibiting this procedure were labeled as sample "G025" (where Ge was evaporated with shorter duration) and sample "G050" (where Ge was evaporated with longer duration).

– As for the top capping Si_3N_4 layer, the standard LPCVD process at 810^OC was applied, resulting in stoichiometric silicon nitride layer thickness of 35 nm, as obtained by XTEM.

Five different structures were prepared: two samples with Si NCs (one with smaller and one with expectedly larger Si NCs), two samples with the planned Ge NCs and one additional reference structure which consisted of all other layers except that it does not contain any NCs (no step corresponding to NC formation was inserted into the sample formation).

4.7.1 Transmission electron microscopy study

All samples were examined by high-resolution XTEM with or without energy filtering for Si, N, O, and Ge. It was found that samples "O060" and "Q120" contain Si nanocrystals between two Si_3N_4 layers, as planned (see *Figs. 4−23* and *4−26*).
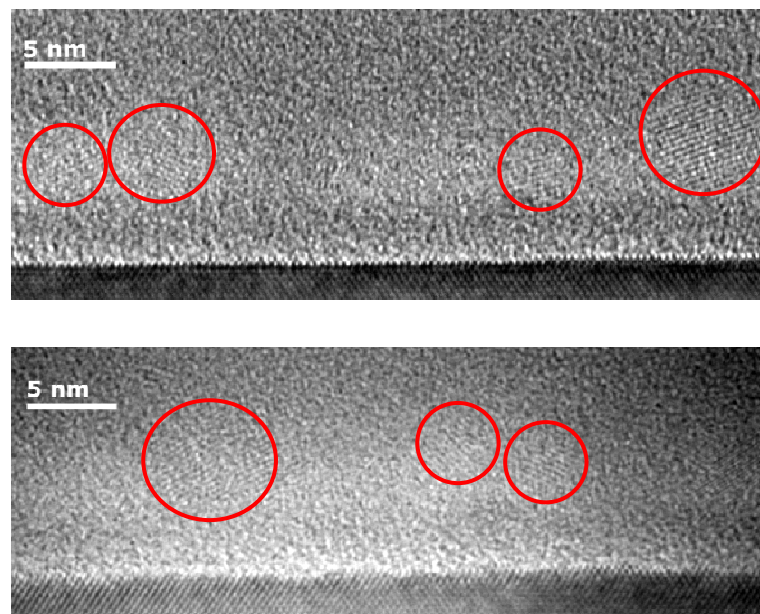
Fig. 4−23. High-resolution XTEM images of sample "O060", indicating existence of Si NCs at a distance of 5–6 nm from the Si substrate (circles indicate the NCs)
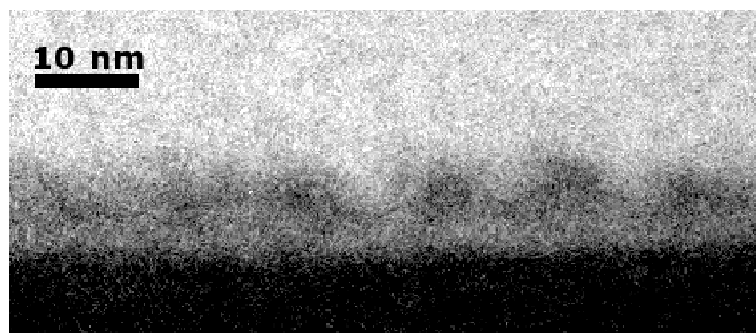
Fig. 4−24. Energy-filtered XTEM image of sample "O060" with white dots corresponding to nitrogen atoms

Fig. 4−25. Energy-filtered XTEM image of sample "O060" with white dots corresponding to silicon atoms

Fig. 4−26. High-resolution XTEM images of sample "Q120", indicating existence of Si NCs at a distance of 5–6 nm from the Si substrate (circles indicate the NCs)

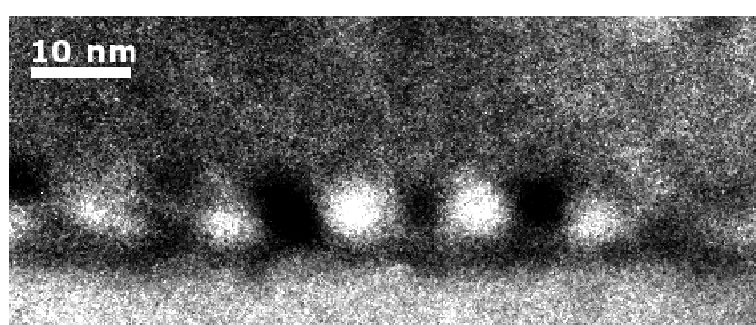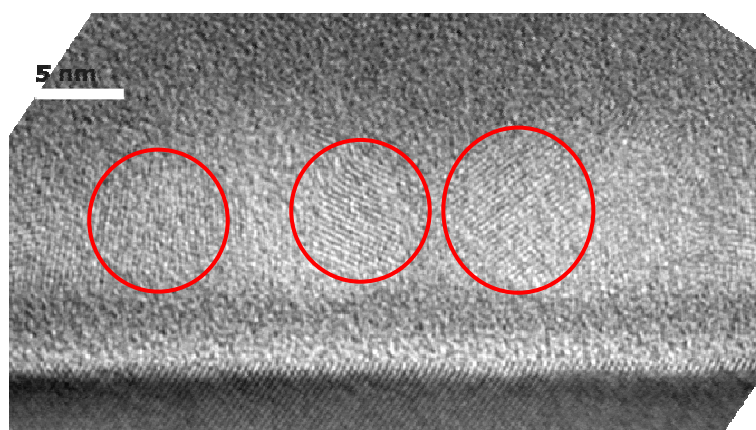*Fig. 4−27. Energy-filtered XTEM image of sample "Q120" with white dots corresponding to nitrogen atoms*

Fig. 4−28. Energy-filtered XTEM image of sample "Q120" with white dots corresponding to silicon atoms
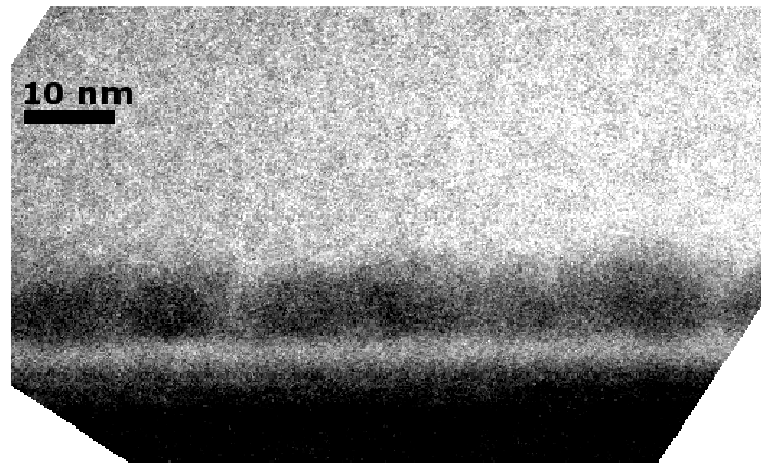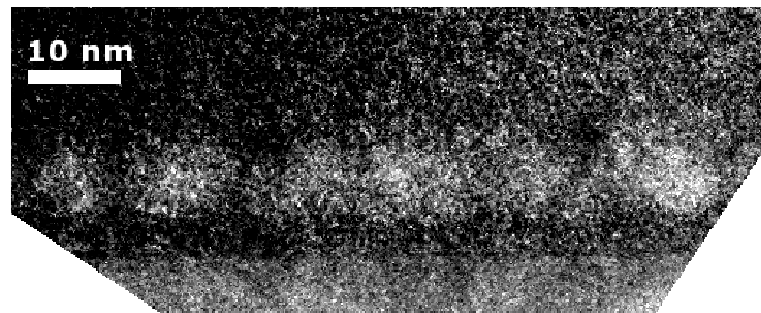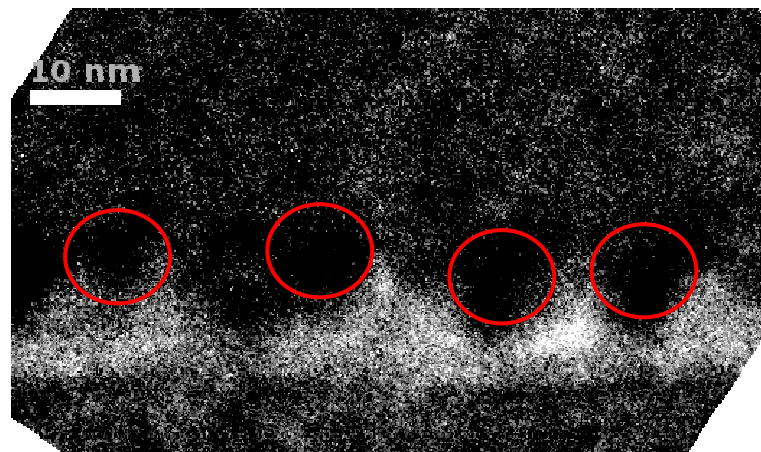

Fig. 4−29. Energy-filtered XTEM image of sample "Q120" with white dots corresponding to oxygen atoms (location of Si NCs indicated by circles). SiO$_x$ "pyramids" are clearly visible between the Si NCs

It is observed that the size and distribution of Si NCs in sample "O060" are in good agreement with those NCs observed in sample NI060 (see *Table 4−5*). It proves the good reproducibility of the method (i.e. high-temperature LPCVD with SiH_2Cl_2 on Si_3N_4 layers) applied for Si NC formation. These NCs are located at a distance of 5–6 nm from the Si substrate, separated from the substrate by a 2.5 nm SiO_2 and a 2.5–3 nm thick Si_3N_4 layer both in samples "O060" and "Q120".

It has been found that the post-oxidation step [BP−8] did not modify the vertical size of the Si NCs in the case of sample "Q120", with respect to sample NI120. However, there is a revealed lateral size shrinkage of the NCs, well indicated by the increased number of "bridges" that separate them from each other, as seen in *Figs. 4−24,4−25,4−27,4−28*. It has been found, that the post-oxidation step formed silicon oxide between and underneath the Si NCs. No silicon oxide was found on top of Si NCs (see *Fig. 4−29*). The lateral size of the Si NCs in the case of sample "Q120" is found to be around 5–6 nm, that does not show substantive difference from NC size determined for sample "O060". It means a nearly identical cross-section of NCs towards the substrate, while the "height" of NCs differ slightly between samples "O060" and "Q120".

As for samples with evaporated Ge, still no evidence was found by XTEM for Ge existence in the layer. On one hand, TEM is a local method (monitoring areas within a few microns), and if the evaporation was laterally inhomogeneous enough, it is possible that Ge is present in the layer but elsewhere.

4.8 Conclusions

In this chapter, the following results concerning the structure of the prepared samples were presented.

Low-pressure chemical vapor deposited SiN_x/nc-Si/SiN_x heterostructures on Si wafers

The effect of the annealing time was investigated on this structure with *spectroscopic ellipsometry*. The Si content of the top layer was significantly affected by the annealing: the ellipsometric compositional study showed smaller amount of Si in the top layer, and larger amount of Si in the bottom layer, as a function of annealing time. The probable explanation is diffusion mechanism of Si from the top to the bottom layer through the middle nc-Si layer. Annealing also affected the grain size of the middle nc-Si layer (i.e. it formed larger grains). XPS confirmed the increase of the Si content of the bottom layer with annealing, and XTEM confirmed the increase of grain size in the middle layer. It was also found that the stoichiometry of the bottom SiN_x layer also affects the growth of the nc-Si layer (i.e. the same deposition circumstances result thinner nc-Si layer on Si-rich nitride). [BP−10,BP−11]

Decomposition of the dielectric function of Si with different crystallinity, according to Adachi's Model Dielectric Function

The dielectric functions of crystalline, fine-grained polycrystalline and amorphous Si (all taken from the literature) were decomposed according to Adachi's Model Dielectric Function. The corresponding oscillator parameters were obtained by model fitting to the dielectric function of these three materials. Systematic changes between the three silicon crystalline phases were found in the following parameters: the amplitude of the resonant peak near 4.2 eV (a harmonic oscillator), and the broadenings of resonant peaks near 3.3 and 4.2 eV (excitonic and a 2D resonance, respectively). [BP−3]

Low-pressure chemical vapor deposited Si_3N_4/nc-Si/Si_3N_4 heterostructures on Si wafers

The effect of the nanocrystal size was studied on the dielectric function of the nanocrystalline layer in the optical model, by *spectroscopic ellipsometry*. It was found that those parameters exhibited correlation with the nanocrystal size in the studied samples that were sensitive to the change in the crystallinity of silicon. The transition of the dielectric function of the nc-Si layer from large nanocrystals to smaller nanocrystals was agreeable to the transition of the dielectric function of reference materials with different crystallinity from the crystalline to the amorphous phase. [BP−3]

These structures were also examined by *cross-sectional transmission electron microscopy*. Dependence of the Si nanocrystal size and density on the deposition time was determined. It was found that separated nanocrystals form for deposition times below 120 sec and the barrier between the NCs is the Si_3N_4. Both the size and density of Si NCs were found to increase with increasing deposition time between 30 and 120 sec. [BP−1,BP−3]

Electron-beam evaporated Ge nanocrystals on top of SiO_2 covered Si wafers

These structures were examined by *atomic force microscopy* (AFM) and *scanning electron microscopy* (SEM). The size and lateral density of nanocrystals were obtained by the AFM. It was found that the growth mechanism for the nanocrystals is the Volmer-Weber type. SEM investigation revealed coalescence of nanocrystals at certain deposition times. Power function was obtained between the sheet resistance and NC size, in spite of the exponential dependence reported in the literature. [BP−2]

Low-pressure chemical vapor deposited Si nanocrystals in SiO_2/nc-Si/Si_3N_4 heterostructures on Si wafers

These structures were examined by *X-ray photoelectron spectroscopy* (XPS). XPS showed indication of Si NC existence between the Si_3N_4/SiO_2 interface. Samples with longer Si NC deposition time showed larger concentration of Si NCs than samples with shorter deposition time. [BP−10,BP−11]

Based on the *cross-sectional transmission electron microscopy* study, a *critical thickness* of the nc-Si layer (around 20 nm) is suggested, at which the Si NCs are enabled to form. If the deposition time is increased, this step is followed by the formation of further Si NCs with sizes around this critical thickness until a continuous layer is formed. It means, that with increasing deposition time, the mean size of the Si NCs remains at the critical level, but with increasing density.

Nitric acid-oxidized LPCVD Si nanocrystals between Si_3N_4 layers in Si_3N_4/nc-Si/Si_3N_4/SiO_2 heterostructures on Si wafers

These structures were examined by *cross-sectional transmission electron microscopy* (XTEM) and energy-filtered XTEM (EFTEM). It was found that the oxidation step [BP−8] formed SiO_x "pyramids" between the Si NCs. The SiO_x was found to be present between and below the NCs, however, no oxygen atoms were found above the NCs by EFTEM. The lateral size of Si NCs was significantly modified due to the oxidation, however, no change of the vertical size was observed. The lateral Si NC size of samples with 120 sec deposition time and further oxidation was found to be similar to that of samples with Si NC deposition for 60 sec and no oxidation. It opened the possibility to examine samples with similar lateral, but with different vertical NC size.

Chapter 5 – Results of the memory measurements

5.1 C–V hysteresis

Charging ability was determined by C–V hysteresis and memory window measurements. In the followings, the obtained results and their suggested explanations are described.

It has been found that the hysteresis strongly depended on the applied maximum voltage limit. In *Fig. 5–1*, a C–V hysteresis measurement on sample NI060 with successively increasing limits from ±5 V to ±15 V, step by 1 V, and an additional hysteresis measurement with limits of ±20 V is shown. *Fig. 5–2* shows clearly that the experimental C–V hysteresis width (i.e. the total injected charge in the layer) is an exponential function of the applied voltage limits between 7 V and 14 V.

For comparison, C–V hysteresis is shown for sample NI030 in *Fig. 5–3* between ±10V. It is seen that the maximum insulator capacitance is increased with respect to sample NI060. It is apparent that this is a consequence of the thinner Si NC layer present in this sample. A C–V hysteresis width of 3.7 V was obtained for applied voltage between limits ±10 V. It indicates better charging properties for sample NI030 (sample with smaller Si NCs) than for sample NI060 (sample with larger Si NCs).
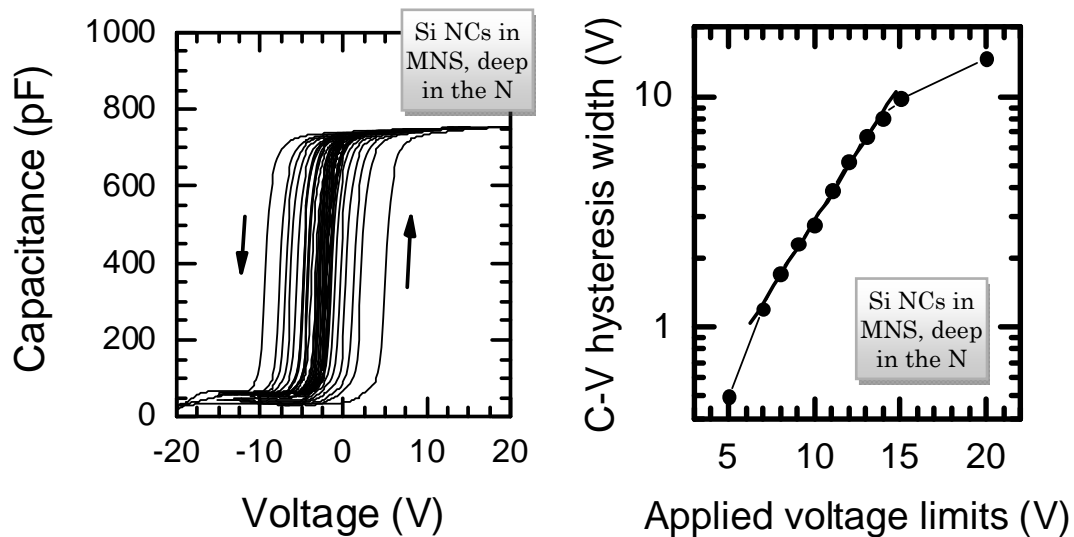
Fig. 5–1. C–V hysteresis of Sample NI060

Fig. 5–2. C–V hysteresis width of Sample NI060 as a function of applied voltage limit

However, as for sample NI000 (see *Fig. 5–4*), the width of the C–V hysteresis between ±10 V is found to be even higher, 4.4 V. This indicates a huge amount of defects in

the Si₃N₄ layer that, as seen, can be charged with small and slow voltages. The saturation of the flat-band voltage shift could be achieved above 20 V.
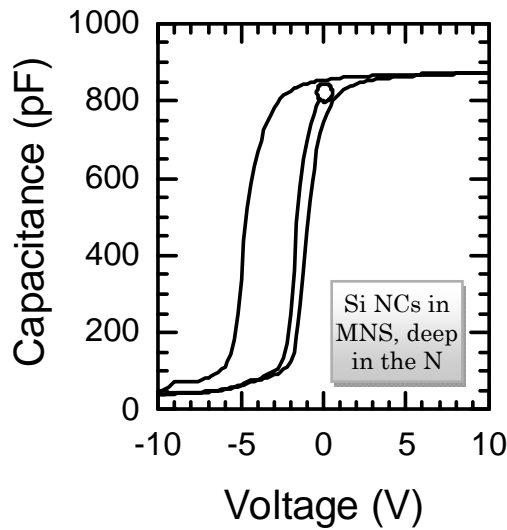
Fig. 5–3 C–V hysteresis of sample NI030   *Fig. 5–4. C–V hysteresis of sample NI000*
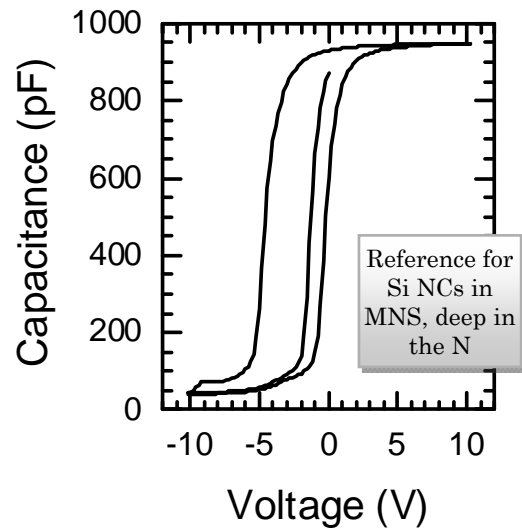
Typical C–V characteristics of MNOS structures with thin chemical oxide tunnel layer COA00 and COA30 without NC deposition and NC deposition time of 30 s, respectively, and of MNS structures with Si₃N₄ tunnel layer NI000 and NI030 without NC deposition and NC deposition time of 30 s, respectively, obtained for the bias range of ±10 V are presented in *Figs. 5–5 a,b*.

Table 5–1. Flat-band voltage shift obtained by capacitance-voltage measurements for bias range of ±10 V

Tunnel layer	Duration of Si NC deposition		
	0 s	30 s	60 s
Thin chemical SiO₂	4.9 V	4.9 V	4.8 V
LPCVD Si₃N₄	4.4 V	3.8 V	2.9 V

Fig. 5−5. Typical C−V characteristics of MNOS (a) and MNS (b) structures between bias range of ±10 V

The flat-band voltage shifts obtained in other structures for bias range of ±10 V are presented in *Table 5−1*. The highest shift of 4.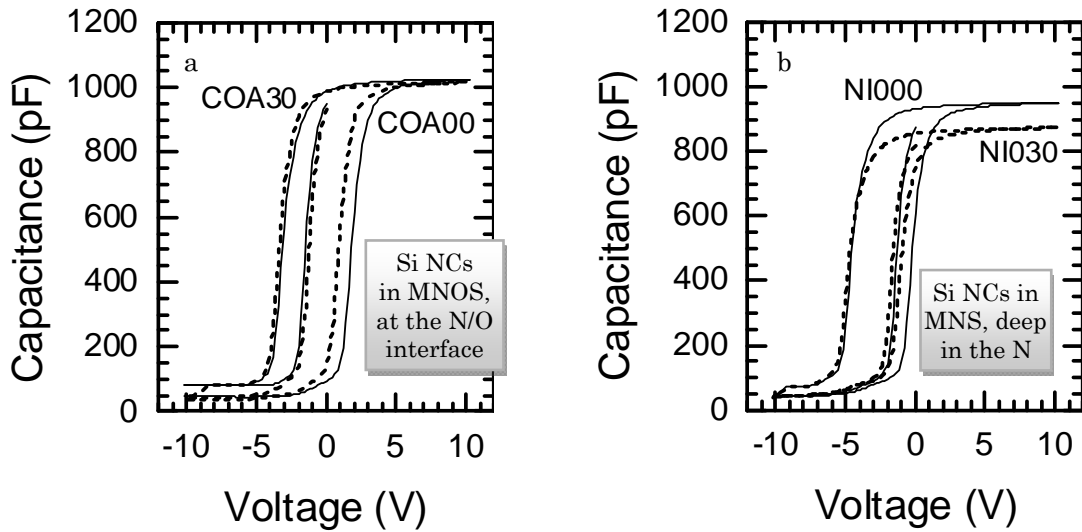8−4.9 V was obtained for structures with the thin chemical oxide, independent of the presence and deposition time of the Si NC layer. For Si_3N_4 tunnel layers the flat-band voltage shift decreased with increasing deposition time from 4.4 V to 2.9 V (the proposed mechanism driving this phenomena is described in the next section). So, according to C−V measurements, the structures with thin chemical tunnel oxide layer exhibited better charging behavior.

That is why further samples "O060" and "Q120" (described in chapter 4.6) were prepared with a thin chemical tunnel oxide layer. C−V hysteresis of these samples with their appropriate reference sample is shown in *Fig. 5−6*. The C−V hysteresis widths and the appropriate insulator capacitances are also indicated in the figure. It is obvious that the distance ~5 nm of the NCs from the substrate enabled highly-efficient tunneling of charge carriers which resulted in extremely wide hysteresis widths (10.3 V for ±10 V voltage ranges) both for samples "O060" and "Q120". However, the low-slope part of the curves corresponding to these samples (on the right side of the hysteresis) indicates high leakage currents, that predict low efficiency of charge storage in these cases. The fact that C−V hysteresis size is so similar between samples "O060" and "Q120" suggests that charge storage takes place in regions (inside the NC, or at the NC/dielectric interface) close to the substrate, because the cross-section of NCs is similar here.

The insulator capacitance of the reference (~1090 pF) is in correspondence with the ~35 nm thickness of the top Si_3N_4 layer of these structures, obtained by ellipsometry and XTEM (see section 4.7). The other two samples that consist NCs have lower insulator capacitance which is in correspondence with the fact that the overall thickness of layers for these samples are larger. The fact that sample "Q120" has smaller insulator capacitance

confirms that characteristic vertical NC size is larger in this structure than in sample "O060".
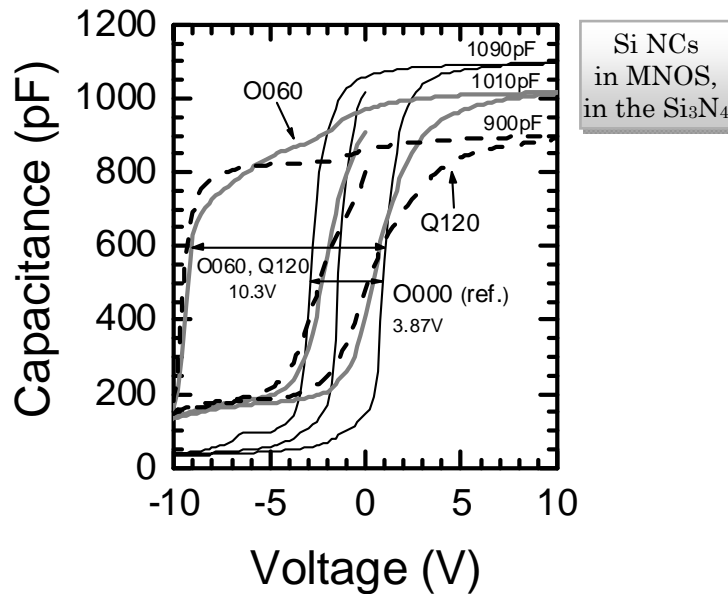
Fig. 5−6. C−V hysteresis curves of MNOS structures with Si NCs at ~5 nm distance from the Si substrate (samples "O060" and "Q120" and their appropriate reference sample O000)
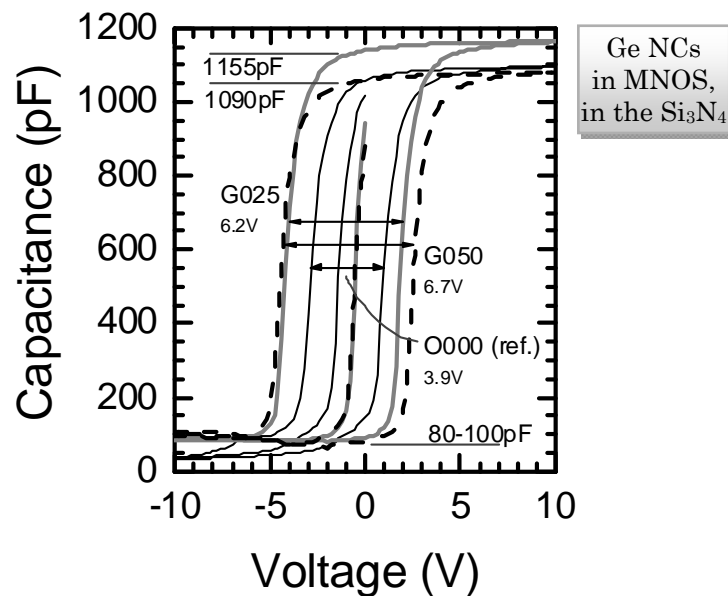
Fig. 5−7. C−V hysteresis of samples with evaporated Ge (samples "G025" and "G050" and appropriate reference sample O000)

As a matter of fact, samples with evaporated Ge (samples "G025" and "G050") also showed improved charging ability compared to their reference, as revealed by C−V

hysteresis measurements (see *Fig. 5−7*). There is a factor of 1.6–1.8 between the amount of trapped charge in samples "G025" or "G050", and their reference. It could indicate either the presence of Ge in the structure (despite the lack of its observation by XTEM), or the structural changes of the SiO_2 surface due to Ge evaporation.

5.2 Memory window

5.2.1 Variation of the charging voltage pulse amplitude

Memory window measurements were performed as a function of the applied charging voltage pulse amplitude and width. Emphasis was taken on suggesting a writing/erasing (W/E) voltage pulse for the possible device operation, at which the disturbance effect of the reading voltage can be eliminated. It is well known, that generally, the measurement disturbs the measurable object in any case, which effect seriously limits the maximum read-cycles of the device, mainly because of leakage (or charging) currents during reading. One of the goals was to keep this leakage current as low as possible.

Memory window widths obtained in MNS samples are shown in *Fig. 5−8*. As the bottom Si_3N_4 layer is rather thick (about 15 nm), the actual injection mechanism is either the Fowler-Nordheim or the trap-assisted tunneling to the conduction or valence band of Si_3N_4 (for positive or negative charging pulses, respectively) [1−21]. Fowler-Nordheim tunneling is a fundamental conduction mechanism for thick insulator layers [5−1,1−22], depending principally on the effective mass of charge carriers and the barrier height at the insulator/substrate interface. NCs are estimated to represent trap sites with 2 eV barrier height for the ground-state energy level. This value is obtained by taking into account the position of the conduction band of bulk Si and of the conduction band of Si_3N_4 [5−2]. However, an impressive calculation of the size-dependency of the ground-state energy of nanocrystalline Si is presented in Ref. [5−2]. Nevertheless, it suggests an increased barrier with respect to defect states of the nitride that have average barrier height around 1 eV only [5−3].

Consequently, a part of the injected charge is probably captured by traps in the bottom Si_3N_4 layer, but another part, which reaches the layer of Si NCs, can be captured by them. It means that the NCs do play a role in charge storage, and it could result in the monotonous dependence of the memory window width on the Si NC density, as shown in *Fig. 5−8*. Detailed explanation for the suggested model of charge storage in MNS structures is as follows (see *Fig. 5−9*).
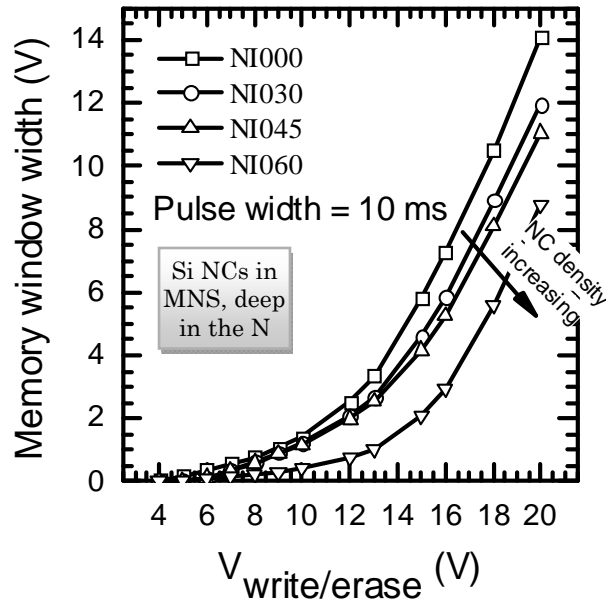
Fig. 5−8. Memory window widths obtained for MNS samples
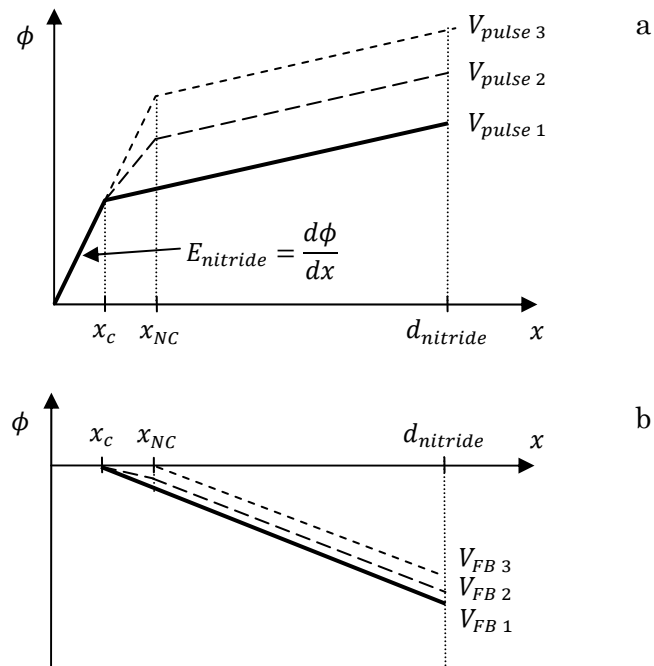
Fig. 5−9. The electrostatic model for the MNS structure with Si NCs: the potential along the cross-section during injection (a) and for flat-band condition (b) for identical electric field at the Si/Si₃N₄ interface during charge injection and the same amount of trapped charge. Thick line corresponds to the case without NCs, the line with short dashes corresponds to the case when only NCs hold the charge, and the line with long dashes represent the case when both nitride traps and NCs hold the charge

In the case when the centroid of charge is closer to the Si surface, than NCs, the memory window width decreases with increasing NC density. If only nitride traps, or only NCs are considered to store the charge (see the thick line, or short dash line in *Fig. 5−9*, respectively), the flat-band voltage (with the use of *Eq. 1−6*) is given by

$$V_{FB} = \phi_{ms} - \frac{Q_t}{\varepsilon_n}(d_n - x),$$ (Eq. 5−1)

where Q_t is the trapped charge density (per unit area), ε_n is the dielectric constant of Si$_3$N$_4$, d_n is the thickness of the Si$_3$N$_4$ layer, and x equals x_c (the distance of the charge centroid from the Si/Si$_3$N$_4$ interface) if no NCs are present in the layer, and x equals x_{NC} (the distance of the NCs from the Si/Si$_3$N$_4$ interface) if the NCs are present in the layer and are responsible for the charge storage only. *Fig. 5−9 b* shows the case when $x = x_c$ with thick line, and the case when $x = x_{NC}$ with short dash line. The absolute value of V_{FB} is higher in the case when only the nitride traps are considered to store the charge ($V_{FB\,1}$), than in the case when only NCs are responsible for charge storage ($V_{FB\,3}$), as seen in *Fig. 5−9 b* and in *Eq. 5−1*. $V_{FB\,2}$ is also shown in the figure, to indicate the intermediate case when both nitride traps and NCs hold the charge.

The potential distribution in the MNS samples with or without Si NCs during negative charging voltage pulses is shown in *Fig. 5−9 a*. *Fig. 5−9 a* suggests that if the NCs are present in the structure, higher voltage pulse is needed to obtain the same electric field at the Si/Si$_3$N$_4$ interface $\left(V_{pulse\,3},\ V_{pulse\,2} > V_{pulse\,1}\right)$. The analytical expression for the charging voltage pulse needed to obtain a certain electric field at the Si/Si$_3$N$_4$ interface is given as

$$V_{pulse} = E_{nitride} \cdot x + \left(E_{nitride} - \frac{Q_t}{\varepsilon_{nitride}}\right) \cdot (d_n - x)$$ (Eq. 5−2)

where x equals x_c (the distance of the charge centroid from the Si/Si$_3$N$_4$ interface) if no NCs are present in the layer, and x equals x_{NC} (the distance of the NCs from the Si/Si$_3$N$_4$ interface) if the NCs are present in the layer and are considered to store the charge only.

In summary, if the NCs participate in charge storage, higher charging voltage and lower flat-band voltage correspond to the same trapped charge and to the same charging electric field (with respect to the case when only nitride traps store the charge). This is the explanation of the decreased memory window width in the case of samples NI030, NI045 and NI060, with respect to sample NI000.

The relative memory window width of this system is shown in *Fig. 5−10*. *The relative memory window width (RMWW) is defined as the memory window width of the sample divided by the memory window width of its reference sample (i.e. the sample without nanocrystals).* It has been found that this plot shows a peak that is thought to correspond to the electronic state (located either inside the NC or at the NC/dielectric interface) where charge carriers are enabled to tunnel into the layer with increased probability (resonant tunneling).
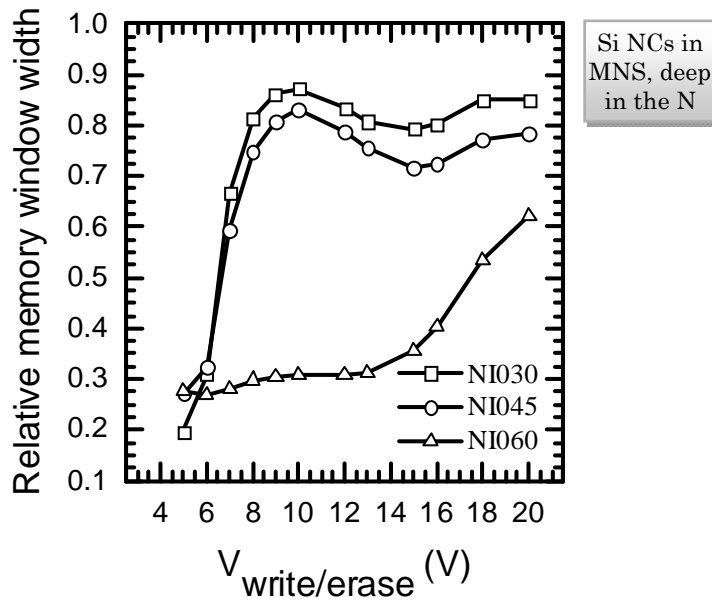
Fig. 5–10. Relative memory window width of the MNS samples NI030, NI045 and NI060

The same phenomena is observed in the case of MNOS structures COA30 and COA60 (with sample COA00 taken as reference), as shown in *Fig. 5–11*. *Fig. 5–12* shows the semi-log representation of the memory window width as a function of the charging pulse amplitude. It reveals that the memory window width of the reference sample (COA00) exhibits strict exponential dependence on the charging pulse amplitude between 7 and 15 V. Taking sample COA30 under consideration, it can be observed that this curve exhibit higher slopes below 10 V, and lower slopes above 10 V (with respect to sample COA00), which strictly lead to the peak at 10 V in the representation shown in *Fig. 5–11*.
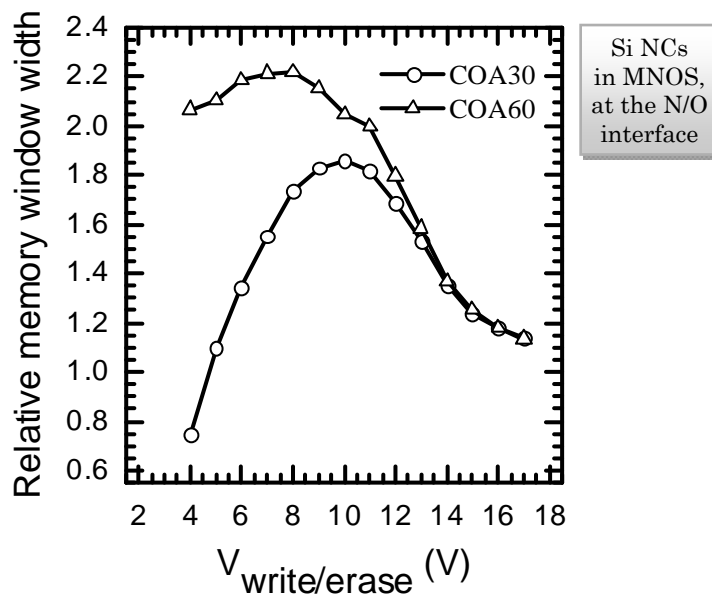
Fig. 5–11. Relative memory window width of the MNOS samples COA30 and COA60
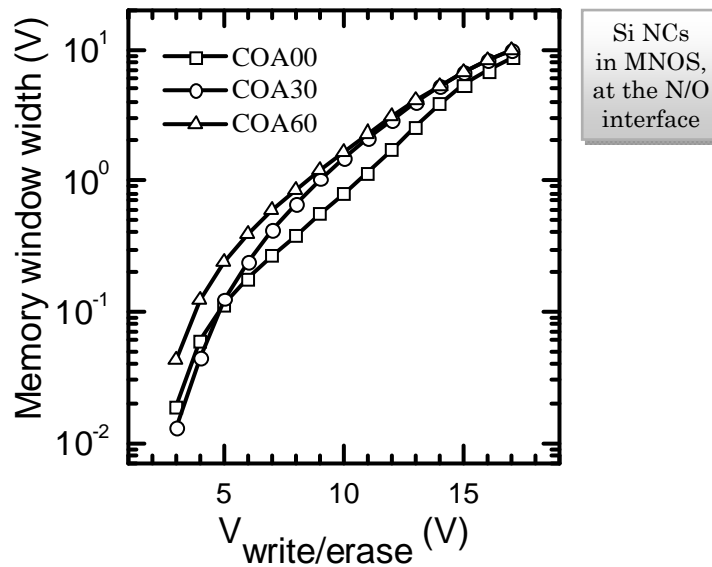
Fig. 5–12. Memory window width of the MNOS samples COA00, COA30 and COA60 as a function of the charging pulse amplitude

Memory window width of samples O060 and Q120 showed similar dependence on the charging pulse amplitude above 6 V (see *Fig. 5–13*), however, below 6 V sample Q120 exhibited better charging behavior. Both samples showed significantly better charging abilities than their appropriate reference (sample O000) at all charging pulse amplitude ranges. The RMWW of these two samples showed a peak near 6–7 V only in the semi-log representation (see *Fig. 5–14*).
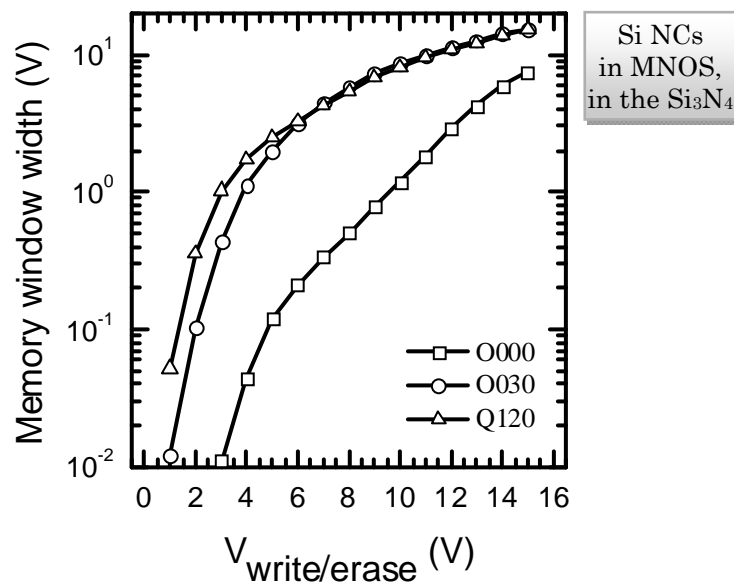
Fig. 5–13. Memory window width of the MNOS samples O000, O060, and Q120 as a function of the charging pulse amplitude
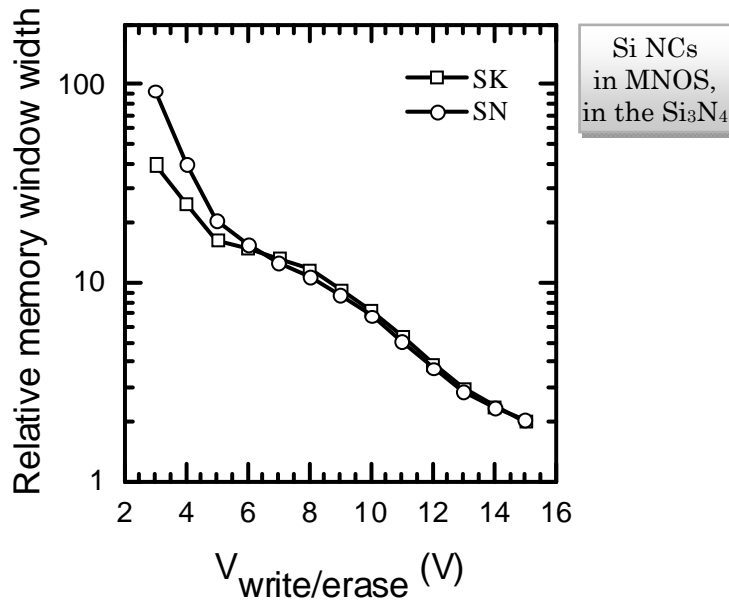
Fig. 5-14. Relative memory window width of the MNOS samples O060 and Q120

Similar peak is observed in the case of samples G025 and G050 between 2.5–3 V, as shown in *Figs. 5-15* and *5-16*. The figures show a slight shift of the peak towards higher voltage, as a result of wider charging pulses. This shift and the narrow sharp peaks themselves suggest a resonant effect probably due to resonant tunneling of carriers to NCs. Another effect of the change of pulse width is the saturation of RMWW above 5 V. It could indicate increased importance of charge loss from traps during the application of the pulse, in the case of longer pulse widths.
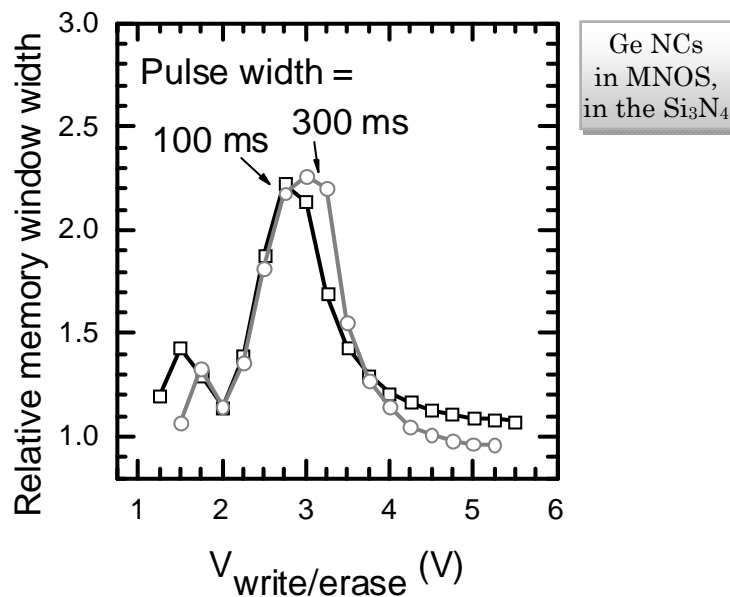
Fig. 5-15. Relative memory window width of MNOS sample G025

Fig. 5–16. Relative memory window width of MNOS sample G050

5.2.2 Variation of the charging voltage pulse duration

The dependence of the memory window width as a function of pulse width is shown in *Fig. 5–17* for samples O060 and Q120. It is shown in *Fig. 5–17 b* that the decrease of memory window width with smaller pulse widths is more dramatic in the case of the reference sample than for samples O060 or Q120. This dependence could be best followed in the RMWW (see *Fig. 5–18*). The systematic increase in the relative memory window suggests increasing probability for capturing charge carriers by the NCs in shorter time. This phenomena could be resolved if one assumes that during charging, deeper traps (in our case, the NCs) capture charge carriers first. This is later followed by charge capture in the shallower nitride traps. Electrons captured by the NCs are closer to the substrate, than the centroid of charge trapped in the nitride. This change clearly leads to the increase of the memory window width, according to *Eq. 1–7.* For wider charging pulses a higher part of the charge is captured by nitride traps. This is why the RMWW decreases with increasing pulse width.

The same study was performed on the other two series of samples as well, at charging pulse amplitude of 15 V. The charging phenomena obtained for samples O060 and Q120 (see *Fig. 5–18*) has not been obtained for MNS samples NI030, NI045, nor NI060 (see *Fig. 5–19 b*). The reason for the lack of this observation is as follows. The bottom Si_3N_4 layer in this series of samples is rather thick (~15 nm), which makes the Fowler-Nordheim or the trap-assisted tunneling to the conduction or valence band of Si_3N_4 as actual injection mechanism (as mentioned earlier). Consequently, the contribution of the most effective direct tunneling is negligible, and charge carriers reach the NCs through the conduction band of Si_3N_4.

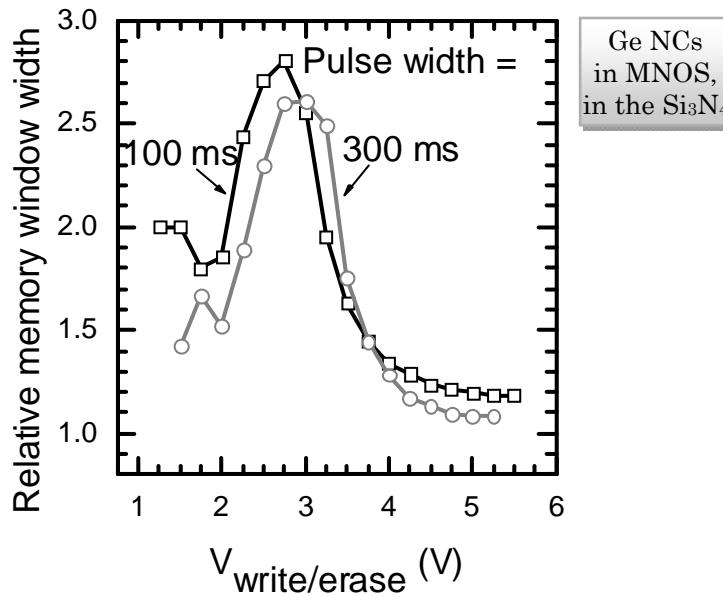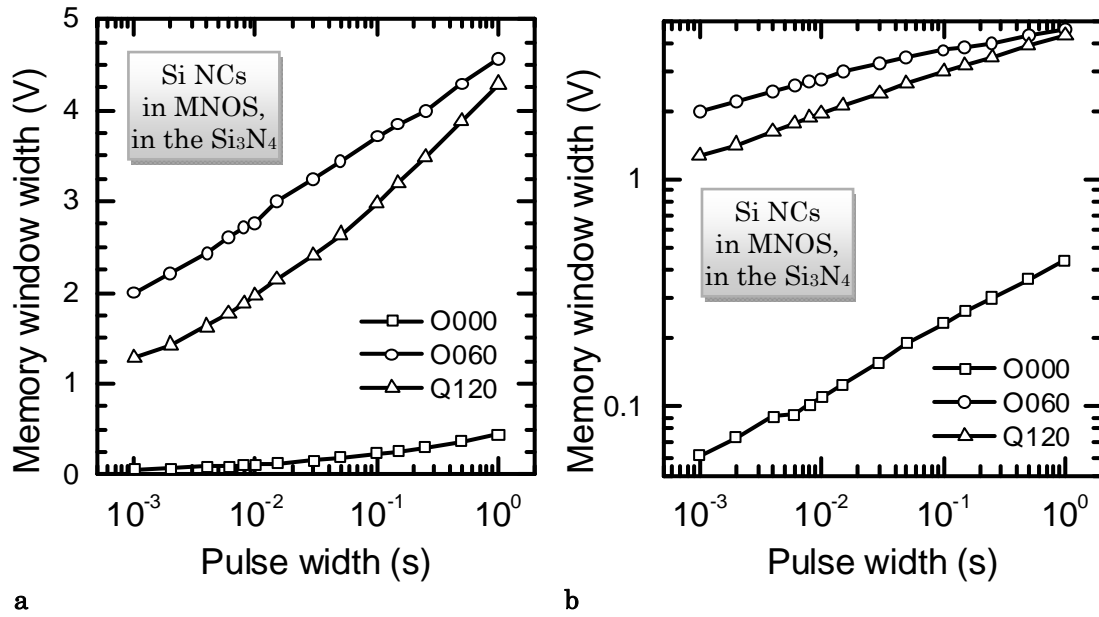Fig. 5–17. Memory window width of samples O000, O060 and Q120 as a function of charging pulse width at pulse amplitude of 5 V, on semi-log (a) and log-log (b) plot
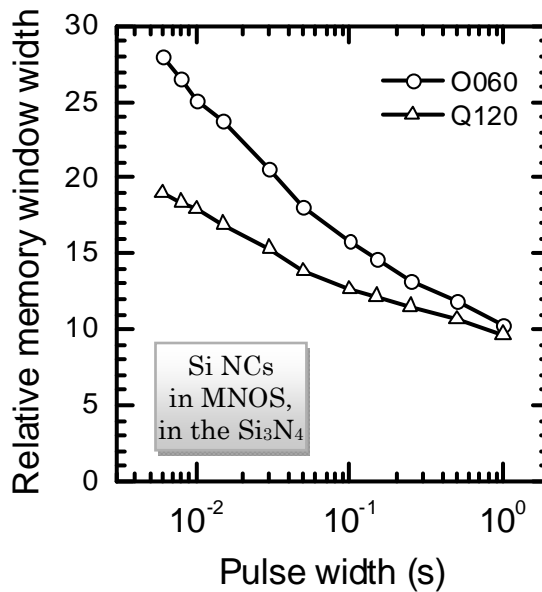
Fig. 5–18. Relative memory window width of samples O060 and Q120 as a function of charging pulse width, at pulse amplitude of 5V

The thin 2.5 nm-thick bottom SiO_2 layer in the case of MNOS samples COA30 and COA60 enables direct tunneling, and this phenomena is visible in *Fig. 5–20 b*. As the charging ability is systematically better for samples COA30 and COA60, with respect to sample COA00, it proves the presence of excess states (the NCs) near the SiO_2/Si_3N_4 interface.

Fig. 5−19. Memory window width of MNS samples NI000, NI030, NI045 and NI060 as a function of charging pulse width, at pulse amplitude of 15 V (a) and relative memory window width of samples NI030, NI045 and NI060 at the same pulse amplitude, as a function of pulse width (b)
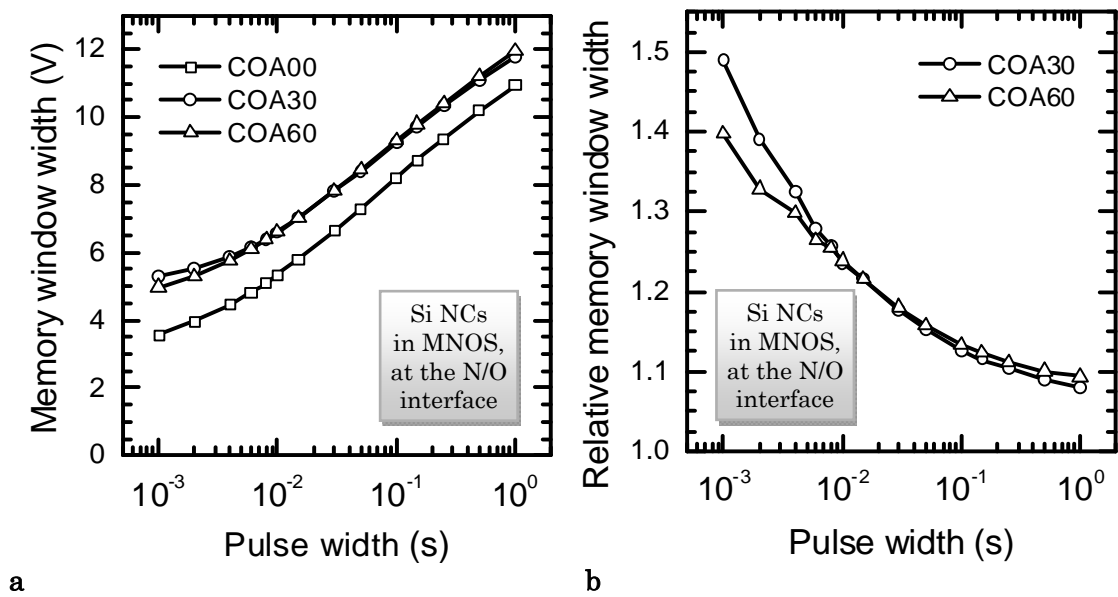
Fig. 5−20. Memory window width of MNOS samples COA00, COA30 and COA60 as a function of charging pulse width, at pulse amplitude of 15 V (a) and relative memory window width of samples COA30 and COA60 at the same pulse amplitude, as a function of pulse width (b)
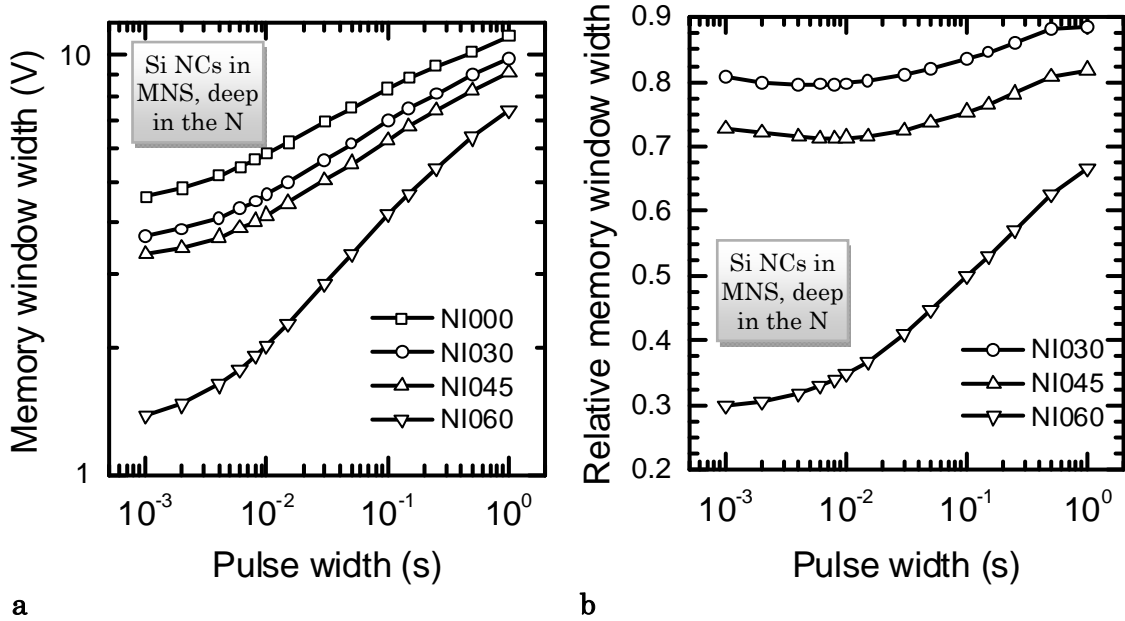
5.2.3 Position of the flat-band voltage as a function of charging pulses

The position of flat-band voltages is shown in *Fig. 5–21* for MNS (NI000, NI030, NI045 and NI060) and MNOS (COA00, COA30, COA60) samples. It has been obtained that the position of the initial flat-band voltage (at zero memory window width) varies from sample to sample, which makes the comparison of samples in this representation rather difficult. Consequently, the flat-band voltage shift (the actual position of the flat-band voltage minus its initial value) versus the charging voltage pulse amplitude plot is used instead (*Fig. 5–22*).

In the case of MNS samples (*Fig. 5–22*) samples containing NCs (NI030, NI045 and NI060) exhibited systematic dependence on the charging voltage, both in positive, and in negative direction of the flat-band voltage shift. The decrease of flat-band voltage shift for both polarities can be explained by that a part of the charge is captured by nitride traps and the other part by NCs. NCs are located deeper from the Si substrate, than charge in nitride traps, as outlined above.

a   b
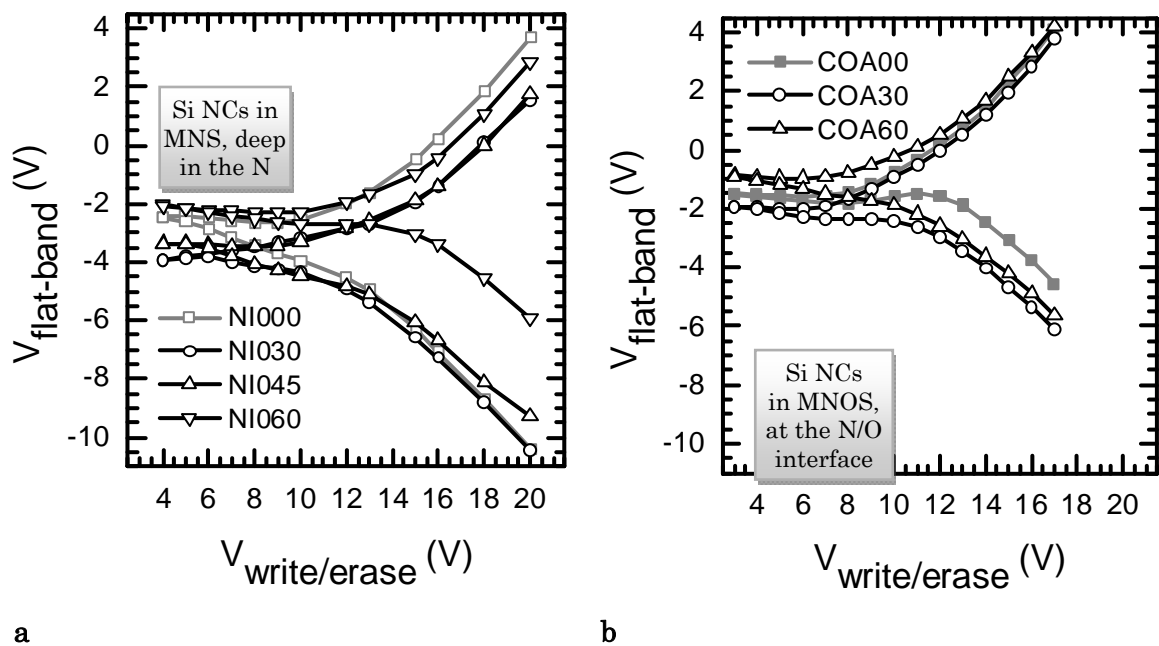
Fig. 5–21. The position of flat-band voltages for MNS (NI000, NI030, NI045 and NI060) and MNOS (COA00, COA30, COA60) samples as a function of charging voltage pulse amplitudes

As for the MNOS structures with Si NCs (Fig. 5–23), clear difference between the samples is only present in the negative direction, while for positive charging pulses, all three samples show similar flat-band voltage shifts. In this case, the NCs are relatively close to the Si substrate (the NC–Si distance is around 2.5 nm for the MNOS, while it is around 15 nm for the MNS samples). It enables direct tunneling to the NCs, which dominates the charging processes of the layer. It means that the relative importance of the

density of the NCs is increased, with respect to the previous structure. Based on the growth model for Si NCs on SiO_2 (see section 4.5), it can be stated that the density of the NCs in sample COA60 is higher than in sample COA30, which results in an increased number of states at the SiO_2/Si_3N_4 interface (corresponding to the larger density of the NCs) in the case of sample COA60. It means larger stored charge in the case of an applied voltage, resulting in higher flat-band voltage shift in the negative direction in the case of sample COA60, with respect to COA30 and COA00 (as shown in *Fig. 5-23*).
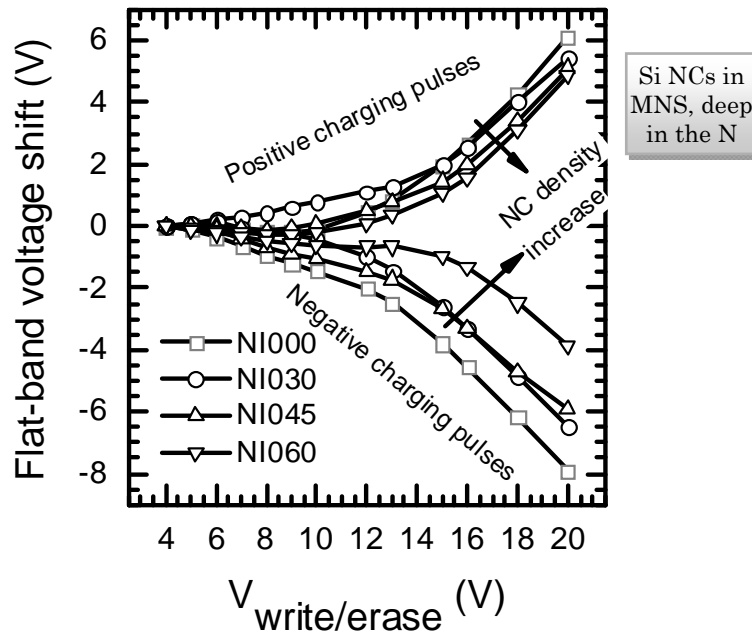
Fig. 5-22. Flat-band voltage shifts for MNS (NI000, NI030, NI045 and NI060) samples as a function of charging voltage pulse amplitudes

Fig. 5-24 shows the flat-band voltage shifts for samples O060, Q120, and O000 as a function of charging voltages. Based on the flat-band voltage shifts, the similar charging ability of samples O060 and Q120 is evident. It means similar available electronics states in these two samples which indicates similar surface density of NCs. These samples have NCs with similar lateral size, but with different vertical size. This result suggests that the surface density of NCs play more important role in charging than the quantum size effect. However, a question remained unsolved until this point: whether multi-electron storage takes place or not at these measurements. If the answer is yes, it is in contradiction with neglecting the quantum size effect in favor of the surface density when calculating the charge to be stored in the layer.
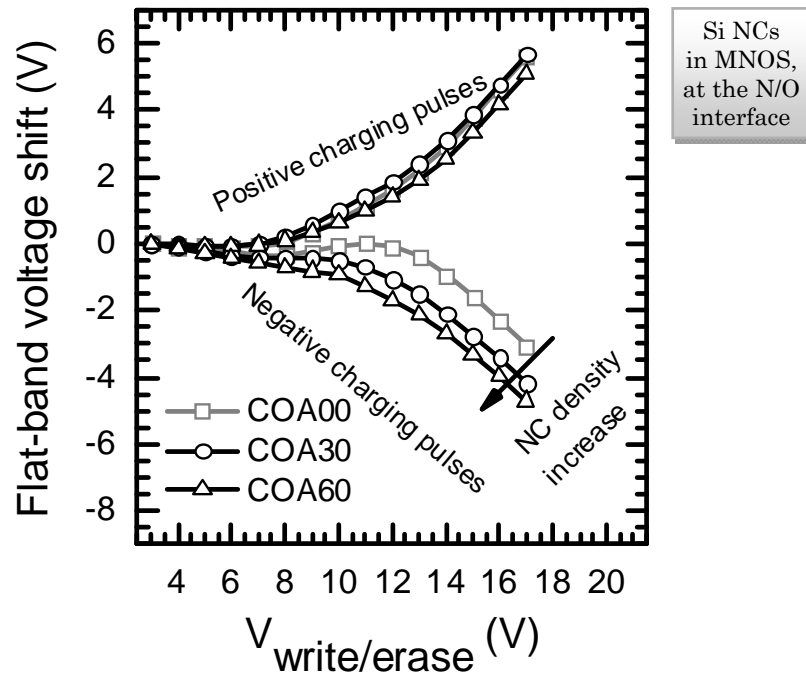
Fig. 5−23. Flat-band voltage shifts for MNOS (COA00, COA30, COA60) samples as a function of charging voltage pulse amplitudes. The nanocrystal density at the SiO_2/Si_3N_4 interface increases from COA30 to COA60
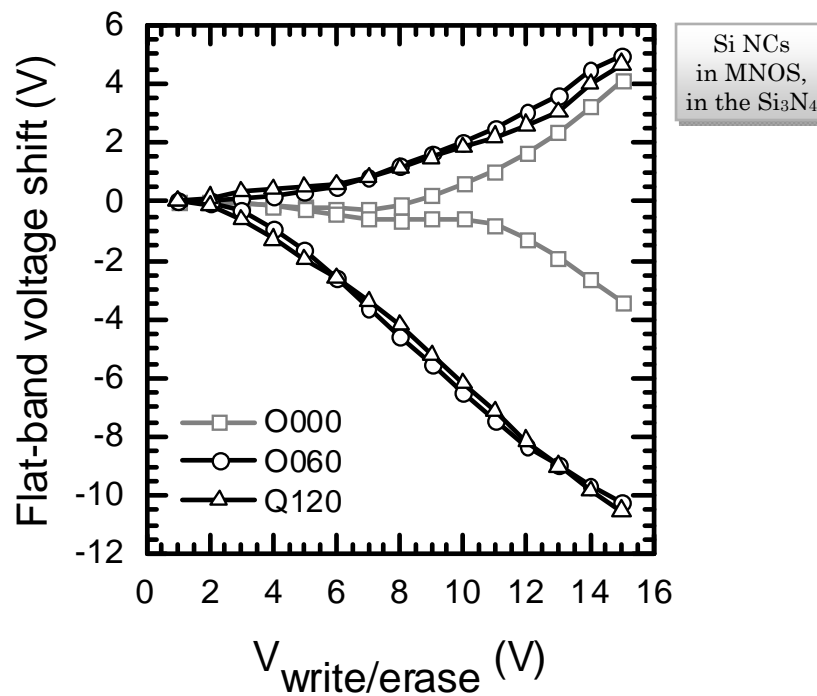
Fig. 5−24. Flat-band voltage shifts for samples O060, Q120, and O000 (reference) as a function of charging voltage pulse amplitudes

5.2.4 Total injected charge

The trapped charge in the layer as a function of the charging voltage is shown for samples O060 and Q120 in *Fig. 5–25*. It is seen, that the order of the trapped charge density reaches the order of the NC density obtained by the evaluation of the XTEM images (~10^{12}/cm^2, see section 4.3) at 10 V and does not change significantly until 15 V. It suggests that multi-electron charge storage is not probable in our case, because the trapped charge density is not significantly higher than the NC density. It means, that one NC stores maximum one electron below charging voltages of 15 V. Therefore, the amount of stored charge is strongly determined by the lateral density of NCs.
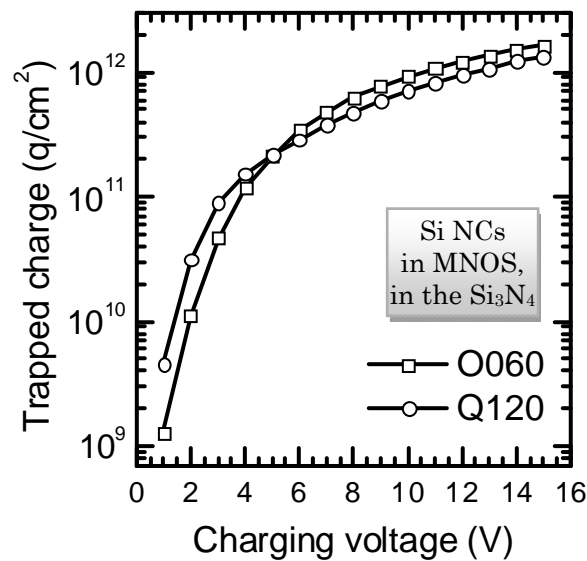
Fig. 5–25. The trapped charge as a function of the charging voltage (for charging voltage pulse duration of 10 ms) for samples O060 and Q120

5.3 Retention

Retention measurements obtained on MNS samples have been published by the author in Ref. [BP−1]. Typical flat-band voltage vs. time and memory window width vs. time dependence of MNS sample NI060 is shown in *Fig. 5−26*. The flat-band voltage vs. time representation consists of two curves: the top curve corresponds to the case of charge loss after a positive charging voltage pulse, while the bottom curve corresponds to the case of a negative charging voltage pulse.

The observed exponential memory window–time dependence was characteristic for all other samples as well, including MNOS structures. Consequently, the parameters of the linear fit for this curve can be used to characterize and distinguish between the samples.

The fitted linear parameters A (axis intercept) and B (slope) for all studied samples (except for samples O060 and Q120) are shown in *Table 5−2* for charging voltages of ±15 V, 10 ms. (Samples O060 and Q120 exhibited fast charge loss.) It should be noted, that the charging voltages for current flash memory chips (those that are used for data storage in pen drives and memory sticks) are in the range of 18–20 V, 300 μs [5−4].
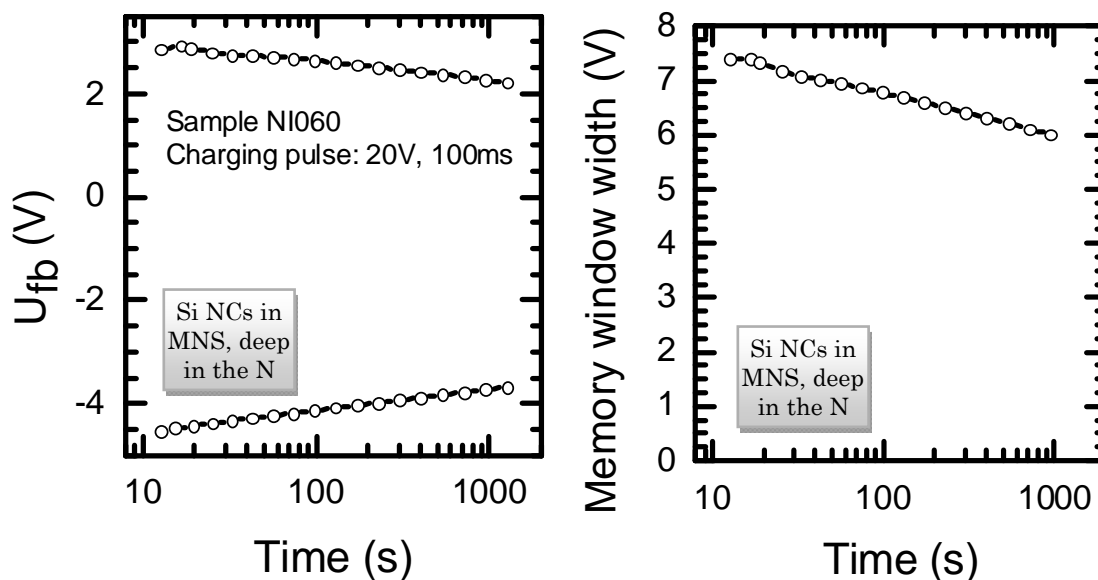
Fig. 5−26. Typical flat-band voltage vs. time and memory window vs. time dependence of MNS sample NI060

Table 5–2. Initial memory window width, linear fit data (axis intercept and charge loss rate {slope}), expected time of disappearance and extrapolated memory window values obtained for the examined MNS and MNOS samples for charging voltages of ±15 V, 10 ms

Sample No.	Memory window width (V)	A–axis intercept (V)	B–slope (V/decade)	Expected disappearance of memory window (years)	Extrapolated memory window width after 1 year (V)	Extrapolated memory window width after 10 years (V)	
NI000	5.80	3.22	-0.444	0.564	0	0	Si NCs in MNS, deep in the N
NI030	4.59	2.30	-0.356	0.091	0	0	
NI045	4.16	1.91	-0.309	0.050	0	0	
NI060	2.06	1.30	-0.204	0.075	0	0	
COA00	5.34	3.97	-0.414	128.29	0.87	0.46	Si NCs in MNOS, at the N/O interface
COA30	6.61	4.79	-0.526	41.19	0.85	0.32	
COA60	6.68	4.52	-0.540	7.37	0.47	0	
O000	7.43	5.79	-0.617	77.07	1.17	0.55	Ge NCs in MNOS, in the Si_3N_4
G025	7.93	5.78	-0.521	3947.98	1.88	1.35	
G050	7.68	5.69	-0.644	21.64	0.86	0.22	

It has been obtained for the MNS samples (samples NI000–NI060) that the size of the NCs strongly affected the retention. Smaller NCs represent smaller barrier for charge carriers, which results in decreased charge storage ability, as indicated by the slopes of the memory window width–time curves. The extrapolated values of the memory window width represent a combination of the initial memory window width and the rate of the charge loss. Based on the linear fit to experimental data, sample NI000 can be extrapolated to keep the injected charge for ~0.56 years, which makes it the most non-volatile structure among the MNS structures, despite its worse charge loss rate. However, if injecting more charge into the layer (with higher and longer charging voltage pulses), sample NI060 becomes the most reliable structure to store the information (see *Table 5–3*).

Fig. 5–27 shows the strong correlation between the initial injected charge in the layer and the charge loss rate (i.e. the "B" parameter of the linear fit) for different samples. Now the main question is the origin of this correlation. Earlier in this chapter, the initial memory window width was found to be a systematic function of the NC size. Based on this result, *Fig. 5–27* suggests a strong correlation between the charge loss rate and the NC size.
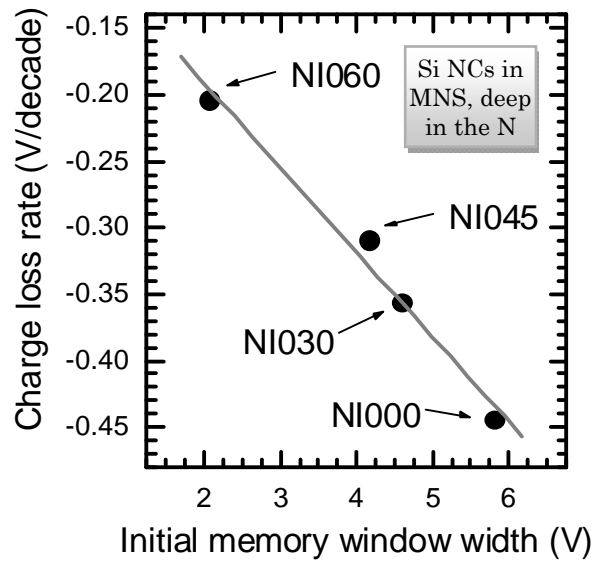
Fig. 5–27. Linear fit for the charge loss rate–memory window width data for samples NI000, NI030, NI045 and NI060, for the case of charging voltages of ±15 V, 10 ms

It was also obtained that the sample with a continuous NC layer (sample NI120) has no memory window after 1 year. It is most probably connected with lateral spreading of the charge after switching off the charging pulse.

Table 5–3. Extrapolated memory window values for 1 year obtained for the examined MNS samples for charging voltages of ±20 V, 400 ms

Sample No.	Extrapolated memory window width after 1 year (V)	Si NCs in MNS, deep in the N
NI000	3.51	
NI030	3.02	
NI045	2.62	
NI060	3.80	
NI120	0	

The MNOS samples (COA00, COA30 and COA60) exhibit similar monotonous dependence of the charge loss rate on the initial injected charge. However, in this case, there is only minor variation of the charge storage (and also the injection) properties of samples COA30 and COA60 as a function of the deposition parameters.

The most reliable memory structure for charging voltages of ±15 V, 10 ms was found to be sample "G025". It has an expected 1.35 V of memory window width after 10 years and 1.88 V after 1 year. Moreover, this sample has a relatively high initial memory window width. Its charge loss rate is better than that of COA samples and worse than the MNS samples.

5.4 Conclusions

In this chapter, the following results concerning the memory properties of the prepared samples were presented.

Similar charging properties were found for MNOS samples with different nanocrystal sizes, but with equivalent nanocrystal density by capacitance–voltage and also by memory window measurements. As multi-electron storage was not probable in the applied charging voltage range, this result suggests that the density of the nanocrystals plays a key role in the charging properties of the examined samples.

The examined MNS samples where the nanocrystal size and density were simultaneously changing, exhibited monotonous dependence in the charging properties on the nanocrystal size (and density) [BP–1]. It was found that sample with NC size of ~2.2 nm (sample NI030) exhibited a C–V hysteresis of 3.7 V, measured between ±10 V, while sample with NC size of ~5.1 nm (sample NI060) exhibited C–V hysteresis of 5.1 V for the same loop. The reference sample NI000 (without nanocrystals) showed also significant C–V hysteresis, which indicated large amount of traps in the Si_3N_4 layer.

The relative memory window width (RMWW) was defined as the ratio of the memory window width of a certain sample with NCs and that of its appropriate reference. It was found that the RMWW increased with decreasing pulse width. This indicates that deeper trap sites represented by the NCs get charged earlier than the shallower nitride traps, which means increased importance of the charge in the NCs if going towards shorter charging pulse widths. The dependence of the RMWW on the charging pulse amplitude was explained by resonant tunneling.

Systematic dependence of the memory window width (flat-band voltage shift) was obtained as a function of the nanocrystal size and density in both the MNS and MNOS samples [BP–1,BP–8], but the dependence was opposite. In the case of MNS structures the memory window width decreased with increasing nanocrystal density. This is due to the fact that nanocrystals are located deeper in the nitride layer than the charge centroid captured by the nitride traps. The strong correlation found between the long-term charge storage property (retention) of the samples and the initial memory window width confirms this explanation. In the case of MNOS structures the memory window width increased with increasing nanocrystal density. This is due to direct tunneling of charge into the nanocrystals.

Summary

My new scientific results are as follows:

1. I have determined a systematic dependence of the Si distribution as a function of high-temperature annealing time in low-pressure chemical vapor deposited SiN_x/nc-Si/SiN_x structures prepared on Si wafers, by spectroscopic ellipsometry. The Si content decreased in the top layer and increased in the bottom layer due to annealing [BP−6,BP−7]. The increase of the Si content in the bottom layer is confirmed by X-ray photoelectron spectroscopy results [BP−10,BP−11]. This indicates the diffusion of Si atoms from the top to the bottom SiN_x layer, through the grain boundaries of the middle nanocrystalline Si layer. During the annealing steps, the middle nanocrystalline Si layer exhibited an increase of the nanocrystal size, as revealed by both ellipsometry and cross-sectional transmission electron microscopy [BP−6,BP−7]. I have observed similar diffusion phenomenon was detected for different structures (Ge-rich SiO_2 layers on top of Si) [BP−4,BP−5].

2. Studying Si_3N_4/nc-Si/Si_3N_4 structures prepared on Si wafers by spectroscopic ellipsometry I have determined that selected oscillator parameters of Adachi's Model Dielectric Function (the strength and broadening parameter of the Damped Harmonic Oscillator at 4.24 eV, and the broadening parameter of all Critical Points at 3.31 eV) exhibited correlation with the nanocrystal size. The transition of the dielectric function of the nanocrystalline Si layer from large nanocrystals to smaller nanocrystals was agreeable to the transition of the dielectric function of reference materials with different crystallinity from the crystalline to the amorphous phase. [BP−3]

3. I have identified the Volmer-Weber type of nanocrystal growth mechanism in the case of electron-beam evaporated Ge nanocrystals on top of SiO_2 covered Si wafers based on the size and density of Ge nanocrystals obtained by atomic force microscopy and scanning electron microscopy. I have determined a systematic dependence between the sheet resistance and NC size. [BP−2]

4. I have obtained that oxidation with nitric acid [BP−8] modifies the lateral size of the Si nanocrystals in the case of low-pressure chemical vapor deposited Si nanocrystals [BP−1,BP−13] on Si_3N_4/nc-Si/Si_3N_4/SiO_2/Si structures, as obtained by cross-sectional transmission electron microscopy and energy-filtered cross-sectional transmission electron microscopy. I have found that the oxidation formed SiO_x between the Si nanocrystals, which increased their separation. The SiO_x was found to be present between and below the nanocrystals, and no oxygen atoms were found

above the nanocrystals. This has opened the possibility to examine samples with similar lateral, but with different vertical NC size.

5. I have developed a new method for the flat-band voltage determination [BP−1, BP−8,BP−9,BP−12] for memory window and retention measurements. I have found similar charging properties for MNOS samples with different nanocrystal sizes, but with equivalent nanocrystal density. This result suggested that the density of the nanocrystals plays a key role in the charging properties of the examined samples.

    I have obtained a systematic dependence of the memory window on the nanocrystal density in both the MNS and MNOS samples [BP−1,BP−8], but the dependence was opposite. The explanation for this observation is based on the different distance of the NCs from the Si substrate.

    Defining the relative memory window width (RMWW) as the ratio of the memory window width of a certain sample with NCs and that of its appropriate reference, I have found and explained that the RMWW increased with decreasing pulse width in most of the studied structures. I have explained the dependence of the RMWW on the charging pulse amplitude by resonant tunneling.

Utilization of the new scientific results

The results achieved by the use of spectroscopic ellipsometric measurement and evaluation led to a better understanding of the size dependence of the dielectric function of materials. The developed oxidation method for Si nanocrystals with nitric acid opened a new possibility for size modification of nanoparticles. The development of the measurement method for the flat-band voltage is exploited in the memory window and retention measurements of metal–insulator–semiconductor (MIS) memory structures. The suggested relative memory window width representation opened a new way of evaluation of experimental results, e.g., for the examination of the resonant tunneling phenomena in MIS memory structures. The obtained results on memory behaviour led to a better understanding of charge injection and charge storage in MIS memory elements and to the realization of possible ways of improvement.

Until now, I have two independent citations for my publications.

List of publications

This Ph.D. work is based on the following publications:

[BP−1]   P. Basa, Zs. J. Horváth, T. Jászi, A. E. Pap, L. Dobos, B. Pécz, L. Tóth, and
P. Szöllősi, *Electrical and memory properties of silicon nitride structures with
embedded Si nanocrystals*, Physica E **38**, 71–75 (2007)
(Impact factor in 2006: 1.084)

[BP−2]   P. Basa, G. Molnár, L. Dobos, B. Pécz, L. Tóth, A. L. Tóth, A. A. Koós, L. Dózsa,
Á. Nemcsics, and Zs. J. Horváth, *Formation of Ge nanocrystals in SiO₂ by
electron beam evaporation*, Journal of Nanoscience and Nanotechnology **8**,
818–822 (2008) (Impact factor in 2006: 2.194)

[BP−3]   P. Basa, P. Petrik, M. Fried, L. Dobos, B. Pécz, L. Tóth, *Si nanocrystals in silicon
nitride: an ellipsometric study using parametric semiconductor models*,
Physica E **38**, 76–79 (2007) (Impact factor in 2006: 1.084)

[BP−4]   P. Basa, A. S. Alagoz, T. Lohner, M. Kulakci, R. Turan, K. Nagy, Zs.J. Horváth,
*Electrical and ellipsometry study of sputtered SiO₂ structures with embedded Ge
nanocrystals*, Applied Surface Science **254**, 3626–3629 (2008)
(Impact factor in 2006: 1.436)

[BP−5]   P. Basa, P. Petrik, M. Fried, A. Dâna, A. Aydinli, S. Foss, T. G. Finstad,
*Spectroscopic ellipsometric study of Ge nanocrystals embedded in SiO₂ using
parametric models*, Physica Status Solidi C **5**, 1332–1336 (2008)

[BP−6]   P. Basa and P. Petrik, *SiNₓ/nc-Si/SiNₓ multilayers: a spectroscopic ellipsometric
study*, Romanian Journal of Information Science and Technology **8**,
235–240 (2005)

[BP−7]   Zs. J. Horváth, P. Basa, P. Petrik, Cs. Dücső, T. Jászi, L. Dobos, L. Tóth,
T. Lohner, B. Pécz, and M. Fried, *Si nanocrystals in sandwiched SiNₓ structures*,
Proceedings of the First International Workshop on Semiconductor
Nanocrystals, SEMINANO2005, Volume 2, 417–420 (2005)

[BP−8]   Zs. J. Horváth, P. Basa, T. Jászi, A. E. Pap, L. Dobos, B. Pécz, L. Tóth,
P. Szöllősi, and K. Nagy, *Electrical and memory properties of Si₃N₄ MIS
structures with embedded Si nanocrystals*, Journal of Nanoscience and
Nanotechnology **8**, 812–817 (2008) (Impact factor in 2006: 2.194)

[BP−9]   P. Szöllősi, <u>P. Basa</u>, Cs. Dücső, B. Máté, M. Ádám, T. Lohner, P. Petrik, B. Pécz, L. Tóth, L. Dobos, L. Dózsa, and Zs. J. Horváth, *Electrical and optical properties of Si-rich SiN$_x$ layers: Effect of annealing*, Current Applied Physics **6**, 179–181 (2006) (Impact factor in 2006: 1.184)

[BP−10]   D. L. Wainstein, A. I. Kovalev, Cs. Dücső, T. Jászi, <u>P. Basa</u>, Zs. J. Horváth, T. Lohner and P. Petrik, *X-ray photoelectron spectroscopy investigations of Si in non-stoichiometric SiN$_x$ LPCVD multilayered coatings*, Physica E **38**, 156–159 (2007) (Impact factor in 2006: 1.084)

[BP−11]   A. I. Kovalev, D. L. Wainstein, D. I. Tetelbaum, A. N. Mikhailov, Y. Golan, Y. Lifshitz, A. Berman, <u>P. Basa</u>, Zs. J. Horvath, *Electron spectroscopy investigations of semiconductor nanocrystals formed by various technologies*, International Journal of Nanoparticles **1**, 14–31 (2008)

[BP−12]   <u>Basa P.</u>, Horváth Zs. J., Jászi T., Molnár G., Pap A. E., Dobos L., Tóth L., Pécz B.: *Nem-illékony nanokristályos félvezető memóriák*, Híradástechnika **62**, 43–46 (2007)

Other publications related to the subject:

[BP−13]   P. Petrik, M. Fried, T. Lohner, N. Q. Khánh, <u>P. Basa</u>, O. Polgár, C. Major, J. Gyulai, F. Cayrel and D. Alquier, *Dielectric function of disorder in high-fluence helium-implanted silicon*, Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms **253**, 192–195 (2006) (Impact factor in 2005: 1.181)

[BP−14]   P. Petrik, M. Fried, É. Vázsonyi, T. Lohner, E. Horváth, O. Polgár, <u>P. Basa</u>, I. Bársony and J. Gyulai, *Ellipsometric characterization of nanocrystals in porous silicon*, Applied Surface Science **253**, 200–203 (2006) (Impact factor in 2005: 1.263)

References

Preface

[0–1]   International Technology Roadmap For Semiconductors 2007 edition, *Process Integration, Devices, and Structures, Non-volatile Memory*, 35–50 (2007) URL http://www.itrs.net

Chapter 1

[1–1]   Wikipedia – The free Encyclopedia URL http://www.en.wikipedia.org and Answers.com – Online Dictionary, Encyclopedia and much more URL http://www.answers.com

[1–2]   S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, *A silicon nanocrystals based memory,* Applied Physics Letters **68**, 1377–1379 (1996)

[1–3]   R. A. Rao, R. F. Steimle, M. Sadd, C. T. Swift, B. Hradsky, S. Straub, T. Merchant, M. Stoker, S. G. H. Anderson, M. Rossow, J. Yater, B. Acred, K. Harber, E. J. Prinz, B. E. White Jr., R. Muralidhar, *Silicon nanocrystal based memory devices for NVM and DRAM applications*, Solid-State Electronics **48**, 1463–1473 (2004)

[1–4]   P. Normand, E. Kapetanakis, P. Dimitrakis, D. Skarlatos, K. Beltsios, D. Tsoukalas, C. Bonafos, G. Ben Assayag, N. Cherkashin, A. Claverie, J.A. Van Den Berg, V. Soncini, A. Agarwal, M. Ameen, M. Perego, M. Fanciulli, *Nanocrystals manufacturing by ultra-low-energy ion-beam-synthesis for non-volatile memory applications*, Nuclear Instruments and Methods in Physics Research B **216**, 228–238 (2004)

[1–5]   P. Normand, E. Kapetanakis, P. Dimitrakis, D. Tsoukalas, K. Beltsios, N. Cherkashin, C. Bonafos, G. Benassayag, H. Coffin, A. Claverie, V. Soncini, A. Agarwal, M. Ameen, *Effect of annealing environment on the memory properties of thin oxides with embedded Si nanocrystals obtained by low-energy ion-beam synthesis*, Applied Physics Letters **83**, 168–170 (2003)

[1–6]   T. Müller, K.-H. Heinig, B. Schmidt, L. Röntzsch, K.-H. Stegemann, *Fabrication of Si nanocrystals for nonvolatile memories using ion beams*, Proceedings of the First International Workshop on Semiconductor Nanocrystals SEMINANO2005, edited by B. Pődör, Zs. J.Horváth, P.Basa, Budapest, Hungary (2005), Vol. 1, pp. 151–156, URL http://www.mfa.kfki.hu/conferences/seminano2005

References

[1−7]   Hiroshi Tsuji, Nobutoshi Arai, Naoyuki Gotoh, Takashi Minotani, Kenji Kojima, Kouichiro Adachi, Hiroshi Kotaki, Toyotsugu Ishibashi, Yasuhito Gotoh, Junzo Ishikawa, *Nanoparticle formation in 25-nm-SiO₂ thin layer by germanium negative-ion implantation and its capacitance–voltage characteristics*, Nuclear Instruments and Methods in Physics Research B **257**, 94–98 (2007)

[1−8]   Kaori Masuda, Masahiro Yamamoto, Masatoshi Kanaya, Yoshihiko Kanemitsu, *Fabrication of Ge nanocrystals in SiO₂ films by ion implantation: control of size and position*, Journal of Non-Crystalline Solids **299–302**, 1079–1083 (2002)

[1−9]   P. K. Giri, R. Kesavamoorthy, S. Bhattacharya, B. K. Panigrahi, K. G. M. Nair, *Simultaneous formation of Si and Ge nanocrystals in SiO₂ by one step ion implantation*, Materials Science and Engineering B **128**, 201–204 (2006)

[1−10]   Takamitsu Kobayashi, Toshiaki Endoh, Hisashi Fukuda,a) Shigeru Nomura, Akira Sakai, Yuji Ueda, *Ge nanocrystals in SiO₂ films*, Applied Physics Letters **71**, 1195–1197 (1997)

[1−11]   Alexander A. Shklyaev, Masakazu Ichikawa, Effect of interfaces on quantum confinement in Ge dots grown on Si surfaces with a SiO₂ coverage, Surface Science **514**, 19–26 (2002)

[1−12]   Scott K. Stanley, Shawn S. Coffee, and John G. Ekerdt, *Influence of Thermal Treatments on the Chemistry and Self-Assembly of Ge Nanoparticles on SiO₂ surfaces*, Materials Research Society Symposium Proceedings **830**, 51–56 (2005)

[1−13]   Fabio Iacona, Giorgia Franzo, Corrado Spinella, *Correlation between luminescence and structural properties of Si nanocrystals*, Journal of Applied Physics **87**, 1295–1303 (2000)

[1−14]   I. Brunets, A. A. I. Aarnink, A. Boogaard, A.Y. Kovalgin, R. A. M. Wolters, J. Holleman, J. Schmitz, *Low-temperature LPCVD of Si nanocrystals from disilane and trisilane (Silcore®) embedded in ALD-alumina for non-volatile memory devices*, Surface & Coatings Technology **201**, 9209–9214 (2007)

[1−15]   T. Baron, F. Mazen, J. M. Hartmann, P. Mur, R. A. Puglisi, S. Lombardo, G. Ammendola, C. Gerardi, *Growth and characterization of LPCVD Si quantum dots on insulators*, Solid-State Electronics **48**, 1503–1509 (2004)

References

[1−16]   R. A. Rao, H. P. Gasquet, R. F. Steimle, G. Rinkenberger, S. Straub, R. Muralidhar, S. G. H. Anderson, J. A. Yater, J. C. Ledezma, J. Hamilton, B. Acred, C. T. Swift, B. Hradsky, J. Peschke, M. Sadd, E. J. Prinz, K. M. Chang, B. E. White Jr., *Influence of silicon nanocrystal size and density on the performance of non-volatile memory arrays*, Solid-State Electronics **49**, 1722–1727 (2005)

[1−17]   Tae-Youb Kim, Nae-Man Park, Kyung-Hyun Kim, Gun Yong Sung, Young-Woo Ok, Tae-Yeon Seong, Cheol-Jong Choi, *Quantum confinement effect of silicon nanocrystals in situ grown in silicon nitride films*, Applied Phyisics Letters **85**, 5355–5357 (2004)

[1−18]   Kwan Sik Cho, Nae-Man Park, Tae-Youb Kim, Kyung-Hyun Kim, Gun Yong Sung, Jung H. Shin, *High efficiency visible electroluminescence from silicon nanocrystals embedded in silicon nitride using a transparent doping layer*, Applied Phyisics Letters **86**, 071909-1–071909-3 (2005)

[1−19]   Kwan Sik Cho, Nae-Man Park, Tae-Youb Kim, Kyung-Hyun Kim, Jae-Heon Shin, Gun Yong Sung, Jung H. Shin, *Erratum: "High efficiency visible electroluminescence from silicon nanocrystals embedded in silicon nitride using a transparent doping layer" [Appl. Phys. Lett. 86, 071909 (2005)]*, Applied Phyisics Letters **88**, 209904-1 (2006)

[1−20]   Y. M. Wan, N. Buffet, K. van der Jeugd, P. Mur, D. Mariolle b, G. Nicotra, S. Lombardo, *Development of silicon nitride dots for nanocrystal memory cells*, Solid-State Electronics **48**, 1519–1524 (2004)

[1−21]   H. E. Maes, R. J. Van Overstraeten, *Low-field transient behaviour of MNOS devices*, Journal of Applied Physics **47**, 664–666 (1976)

[1−22]   A. V. Ferris-Prabhu, *Theory of MNOS Memory Device Behavior*, IBM Journal of Research and Developement **17**, 125–134 (1973)

[1−23]   K. Lehovec and A. Fedotowsky, *Charge centroid in MNOS devices*, Journal of Applied Physics **48**, 2955–2960 (1977)

[1−24]   P. C. Arnett and B. H. Yun, *Silicon nitride trap properties as revealed by charge-centroid measurements on MNOS devices*, Applied Physics Letters **26**, 94–96 (1975)

[1−25]   H. Maes and R. J. Van Overstraeten, *Simple technique for determination of centroid of nitride charge in MNOS structures*, Applied Physics Letters **27**, 282–287 (1975)

References

[1−26]   Semiconductor Glossary URL `http://semiconductorglossary.com`

[1−27]   Tiezheng Lu, *Detailed investigation of the charge storage in size-controlled Si nanocrystals*, Dr.rer.nat. thesis, Martin-Luther-University Halle-Wittenberg, 2007

[1−28]   T. Z. Lu, M. Alexe, R. Scholz, V. Talelaev, and M. Zacharias, *Multilevel charge storage in silicon nanocrystal multilayers*, Applied Physics Letters **87**, 202110-1–202110-3 (2005)

[1−29]   Aykutlu Dana, Imran Akca, Orcun Ergun, Atilla Aydınlı, Rasit Turan, Terje G. Finstad, *Charge retention in quantized energy levels of nanocrystals*, Physica E **38**, 94–98 (2007)

[1−30]   Y. Nakamura, K. Watanabe, Y. Fukuzawa, M. Ichikawa, *Observation of the quantum-confinement effect in individual Ge nanocrystals on oxidized Si substrates using scanning tunneling spectroscopy*, Applied Physics Letters **87**, 133119-1–133119-3 (2005)

[1−31]   A. Nauen, I. Hapke-Wurst, F. Hohls, U. Zeitler, R. J. Haug, and K. Pierz, *Shot noise in self-assembled InAs quantum dots*, Physical Review B **66**, 161303-1–161303-4 (2002)

[1−32]   Min She, *Semiconductor Flash Memory Scaling*, Ph.D. thesis, University of California, Berkeley, 2003

[1−33]   C. Y. Ng, T. P. Chen, P. Zhao, L. Ding, Y. Liu, Ampere A. Tseng, S. Fung, *Electrical characteristics of Si nanocrystal distributed in a narrow layer in the gate oxide near the gate synthesized with very-low-energy ion beams*, Journal of Applied Phyisics **99**, 106105-1–106105-3 (2006)

[1−34]   S. Lombardo, D. Corso, I. Crupi, C. Gerardi, G. Ammendola, M. Melanotte, B. De Salvo, L. Perniola, *Multi-bit storage through Si nanocrystals embedded in SiO₂*, Microelectronic Engineering **72**, 411–414 (2004)

[1−35]   G. Molas, B. De Salvo, D. Mariolle, G. Ghibaudo, A. Toffoli, N. Buffet, S. Deleonibus, *Single electron charging and discharging phenomena at room temperature in a silicon nanocrystal memory*, Solid-State Electronics **47**, 1645–1649 (2003)

[1−36]   *Freescale Manufactures World's First 24-Mbit Silicon Nanocrystal Memory*, **press release** (2005) URL `http://media.freescale.com/ phoenix.zhtml?c=196520&p=irol-newsArticle&ID=831808`

References

[1−37]   *Nonvolatile Memory: More Than A Flash In The Pan*, **technology report** (2003)
URL http://electronicdesign.com/
Articles/Index.cfm?AD=1&ArticleID=5267

[1−38]   URL http://www.memorystrategies.com/report/focused/ nanocrystal.htm

[1−39]   *What's Ahead for the Flash Memory Market?*, **analysis** (2006)
URL http://www.eweek.com/article2/0,1759,2019388,00.asp

[1−40]   URL http://www.hwsw.hu/hirek/35452/
hama_memoriakartya_flash_sandisk_kingston.html

[1−41]   URL http://www.atmel.com

[1−42]   Tuo-Hung Hou, Chungho Lee, Venkat Narayanan, Udayan Ganguly, Edwin Chihchuan Kan, *Design Optimization of Metal Nanocrystal Memory—Part I: Nanocrystal Array Engineering*, IEEE Transactions on Electron Devices **53**, 3095–3102 (2006)

[1−43]   Tuo-Hung Hou, Chungho Lee, Venkat Narayanan, Udayan Ganguly, Edwin Chihchuan Kan, *Design Optimization of Metal Nanocrystal Memory—Part II: Gate-Stack Engineering*, IEEE Transactions on Electron Devices **53**, 3103–3109 (2006)

[1−44]   T. Osabe, T. Ishii, T. Mine, T. Sano, T. Arigane, T. Fukumura, H, Kurata, S. Saeki, Y. Ikeda, K. Yano, *Charge-injection length in silicon nanocrystal memory cells*, Symposium on VLSI Technology, 2004. Digest of Technical Papers, 242– 243 (2004)

[1−45]   H. I. Hanafi, S. Tiwari, I. Khan, *Fast and long retention-time nano-crystal memory*, IEEE Transactions on Electron Devices **43**, 1553–1558 (1996)

[1−46]   R. Ohba, N. Sugiyama, J. Koga, K. Uchida, A. Toriumi, *Influence of channel depletion on the carrier charging characteristics in Si nanocrystal floating gate memory*, Japanese Journal of Applied Physics Part 1 **39**, 989–993 (2000)

Chapter 2

[2−1]   H. Kobayashi, Ashua, O. Maida, M. Takahashi, and H. Iwasa, *Nitric acid oxidation of Si to form ultrathin silicon dioxide layers with a low leakage current density*, Journal of Applied Physics **94**, 7328–7335 (2003)

[2−2]   K. Reichelt, *Nucleation and growth of thin films*, Vacuum **38**, 1083–1099 (1988)

[2‒3]   F. C. Frank and J. H. van der Merwe, *One dimensional dislocations. I. Static theory*, Proceedings of the Royal Society of London. Series A **198**, 205–216 (1949)

[2‒4]   F. C. Frank and J. H. van der Merwe, *One dimensional dislocations. II. Misfitting monolayers and oriented overgrowth*, Proceedings of the Royal Society of London. Series A **198**, 216–225 (1949)

[2‒5]   M. Volmer and A. Weber, Zeitschrift für Physikalische Chemie **119**, *Keimbildung in übersättigten Gebilden*, 277–301 (1926)

[2‒6]   I. N. Stransky and Von L. Krastanov, Akademie der Wissenschaften und der Literatur, Mainz, Mathematisch-naturwissenschaftliche Klasse, Abteil IIb **146**, 797 (1939)

[2‒7]   URL http://en.wikipedia.org/wiki/Stranski-Krastanov_growth

[2‒8]   D. J. Eaglesham and M. Cerullo, *Dislocation-free Stranski-Krastanow growth of Ge on Si(100)*, Physical Review Letters **64**, 1943–1946 (1990)

[2‒9]   Zs. J. Horváth, M. Ádám, I. Szabó, M. Serényi, Vo Van Tuyen, *Modification of Al/Si interface and Schottky barrier height with chemical treatment*, Applied Surface Science **190**, 441–444 (2002)

Chapter 3

[3‒1]   E. D. Palik (Ed.), *Handbook of Optical Constants of Solids*, Academic Press, San Diego, 1998, p. 774.

[3‒2]   T. Lohner, N. Q. Khánh, and Zs. Zolnai, *Spectroellipsometric characterization of ion implanted semiconductors and porous silicon*, Acta Physica Slovaca **48**, 441–450 (1998)

[3‒3]   M. Serényi, M. Rácz, T. Lohner, *Refractive index of sputtered silicon oxynitride layers for antireflection coating*, Vacuum **61**, 245–249 (2001)

[3‒4]   D.E. Aspnes, in: E.D. Palik (Ed.), *Handbook of Optical Constants of Solids*, Academic Press, Boston, 1985 (Chapter 5).

[3‒5]   URL http://inmmc.org/ftp/material

[3‒6]   S. Adachi, *Model dielectric constants of Si and Ge*, Physical Review B **39**, 12966–12968 (1988)

[3‒7]   E. D. Palik (Ed.), Handbook of Optical Constants of Solids, Academic Press, San Diego, 1998, p. 759.

[3–8]   G. E. Jellison Jr., M. F. Chrisholm, S. M. Gorbatkin, Applied Physics Letters **62**, 3348–3350 (1993)

[3–9]   Tabulated at University of Nebrasca-Lincoln (UNL) (multiple data sets fit).

[3–10]   S. Adachi, H. Mori, S. Ozaki, *Model dielectric function for amorphous semiconductors*, Physical Review B **66**, 153201–153204 (2002)

[3–11]   C. A. T. Salama and G. W. Taylor, *Automatic measurement of charge storage in MNOS memory structures*, Journal of Physics E: Scientific Instruments **3**, 558–560 (1970)

Chapter 4

[4–1]   P. J. French, P. M. Sarro, R. Mallé, E. J. M. Fakkeldij, R. F. Wolffenbuttel, *Optimization of a low-stress silicon nitride process for surface-micromachining applications*, Sensors and Actuators A **58**, 149–157 (1997)

[4–2]   K. Kurihara, S. Hikino, S. Adachi, *Optical properties of N^+ ion-implanted and rapid thermally annealed Si(100) wafers studied by spectroscopic ellipsometry*, Journal of Applied Physics **96**, 3247–3254 (2004)

[4–3]   H. Kobayashi, Asuha, O. Maida, M. Takahashi, and H. Iwasa, *Nitric acid oxidation of Si to form ultrathin silicon dioxide layers with a low leakage current density*, Journal of Applied Physics **94**, 7328–7335 (2003)

[4–4]   S. Ecoffey, D. Bouvet, A. M. Ionescu and P. Fazan, *Low-pressure chemical vapour deposition of nanograin polysilicon ultra-thin films*, Nanotechnology **13**, 290–293 (2002)

[4–5]   M. W. Stoker, T. P. Merchant, R. Rao, R. Muralidhar, S. Straub, and B. E. White Jr., *A Model of Silicon Nanocrystal Nucleation and Growth on SiO_2 by CVD*, Materials Research Society Symposium Proceedings **830**, 243–248 (2005)

[4–6]   Tao Feng, Hongbin Yu, Matthew Dicken, James R. Heath, and Harry A. Atwater, *Probing the size and density of silicon nanocrystals in nanocrystal memory device applications*, Applied Physics Letters **86**, 033103-1–033103-3 (2005)

[4–7]   Q. Wan, T. H. Wang, W. L. Liu, and C. L. Lin, *Ultra-high-density Ge quantum dots on insulator prepared by high-vacuum electron-beam evaporation*, Journal of Crystal Growth **249**, 23–27 (2003)

References

[4–8]   C. A. Neugebauer and M. B. Webb, *Electrical Conduction Mechanism in Ultrathin, Evaporated Metal Films*, Journal of Applied Physics **33**, 74–81 (1962)

[4–9]   D. S. Campbell and A. R. Morley, *Electrical conduction in thin metallic, dielectric and metallic-dielectric films*, Reports on Progress in Physics **34**, 283–368 (1971)

[4–10]   J. C. Anderson, *Conduction in thin semiconductor films*, Advances in Physics **19**, 311–338 (1970)

[4–11]   T. Hartman, *Electrical Conduction in Discontinuous Thin Metal Films*, Journal of Applied Physics **34**, 943–947 (1963)

[4–12]   D. S. Herman and T. N. Rhodin, *Electrical Conduction between Metallic Microparticles*, Journal of Applied Physics **37**, 1594–1601 (1966)

[4–13]   A. J. Quinn, P. Beecher, D. Iacopino, L. Floyd, G. De Marzi, E. V. Shevchenko, H. Weller and G. Redmond, *Manipulating the Charging Energy of Nanocrystal Arrays*, Small **1**, 613–618 (2005)

[4–14]   M. A. Rafiq, Y. Tsuchiya, H. Mizuta, S. Oda, Shigeyasu Uno, Z. A. K. Durrani, and W. I. Milne, *Hopping conduction in size-controlled Si nanocrystals*, Journal of Applied Physics **100**, 014303-1–014303-4 (2006)

Chapter 5

[5–1]   C. Y. Ng, T. P. Chen and C. H. Ang, *Dependence of barrier height and effective mass on nitrogen concentration at SiO_xN_y/Si interface and gate oxide thickness*, Smart Materials and Structures **15**, S39–S42 (2006), and references therein.

[5–2]   Masao Iwamatsuy, Makoto Fujiwara, Naohisa Happo and Kenju Horii, *Effects of dielectric discontinuity on the ground-state energy of charged Si dots covered with a SiO_2 layer*, Journal of Physics: Condensed Matter **9**, 9881–9892 (1997)

[5–3]   S. M. Sze, *Current Transport and Maximum Dielectric Strength of Silicon Nitride Films*, Journal of Applied Physics **38**, 2951–2956 (1967)

[5–4]   C. Clementi and R. Bez, *Non Volatile Memory Technologies: Floating Gate Concept Evolution*, Materials Research Society Symposium Proceedings **830**, 13–24 (2005)

List of used acronyms

AFM	atomic force microscopy
CMOS	complementary metal–oxide–semiconductor
CVD	chemical vapor deposition
DCS	dichloro-silane
DRAM	dynamic random access memory
EEPROM	electrically erasable programmable read-only memory
EFTEM	energy filtered transmission electron microscopy
EMA	effective medium approximation
FET	field-effect transistor
FRAM	ferroelectric random access memory
GPS	general positioning system
LPCVD	low-pressure chemical vapor deposition
MDF	model dielectric function
MIS	metal–insulator–semiconductor
MNS	metal–nitride–semiconductor
MNOS	metal–nitride–oxide–semiconductor
MOS	metal–oxide–semiconductor
MP3	MPEG-1 audio layer 3
MRAM	magnetoresistive random access memory
NC	nanocrystal
PDA	personal digital assistant
PECVD	plasma-enhanced chemical vapor deposition
PRAM	phase-change random access memory
RMWW	relative memory window width
SEM	scanning electron microscopy
SRAM	static random access memory
TEM	transmission electron microscopy
W/E	writing/erasing
XPS	X-ray photoelectron spectroscopy
XTEM	cross-sectional transmission electron microscopy

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